4.5.4 – 168 PIN UNBUFFERED SDRAM DIMM FAMILY

CAPACITY—1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 64, 72, OR 80 BITS

DATA CONFIGURATIONS—Four DATA Word configurations are defined:

—64 BIT without PARITY

—72 BIT for PARITY CODES

—72 BIT & 80 BIT for ECC CODES

CONFIGURATION—20 Different Configurations are defined using various combinationa of X1, X4, X8, and X16 memories including 1 & 2 bank configurations, and three configurations for two asymetrical banks.

LOGIC FEATURES—The modules contain a “SERIAL PRESENCE DETECT” feature that supplies encoded values that define the storage capacity, configuration, data word configuration, refresh mode, speed of the module and other characteristics and attributes of the module.

PACKAGE—168 PIN JEDEC DIMM MEMORY MODULE

PIN ASSIGNMENTS—Figs. 4.5.4–A, & 4.5.4–B,

SPD TABLE & INFORMATION—Fig. 4.5.4–C

Comparison of 168 Pin Buffered & Unbuffered DRAM & SDRAM DIMM—Fig. 4.5.4–D

KEYING METHODOLOGY—Fig. 4.5.4–E

PINOUT COMPARISON DRAM & SDRAM DIMM—Fig. 4.5.4–F

SDRAM CLOCK LOADING—Fig. 4.5.4–G

SDRAM CLOCK WIRING—Fig. 4.5.4–H

CONFIGURATION BLOCK DIAGRAM—Figs. 4.5.4–I through 4.5.4–AK

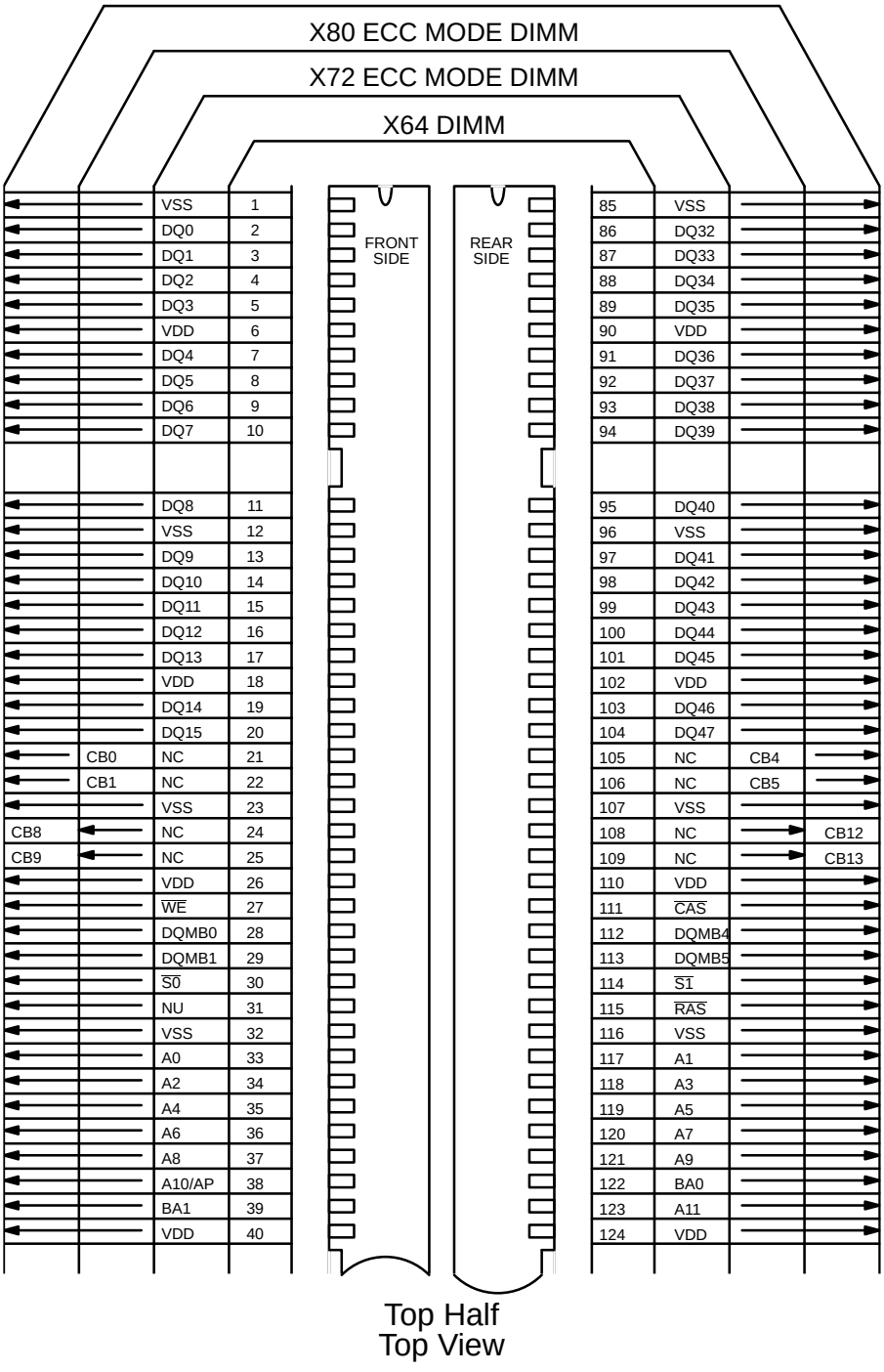
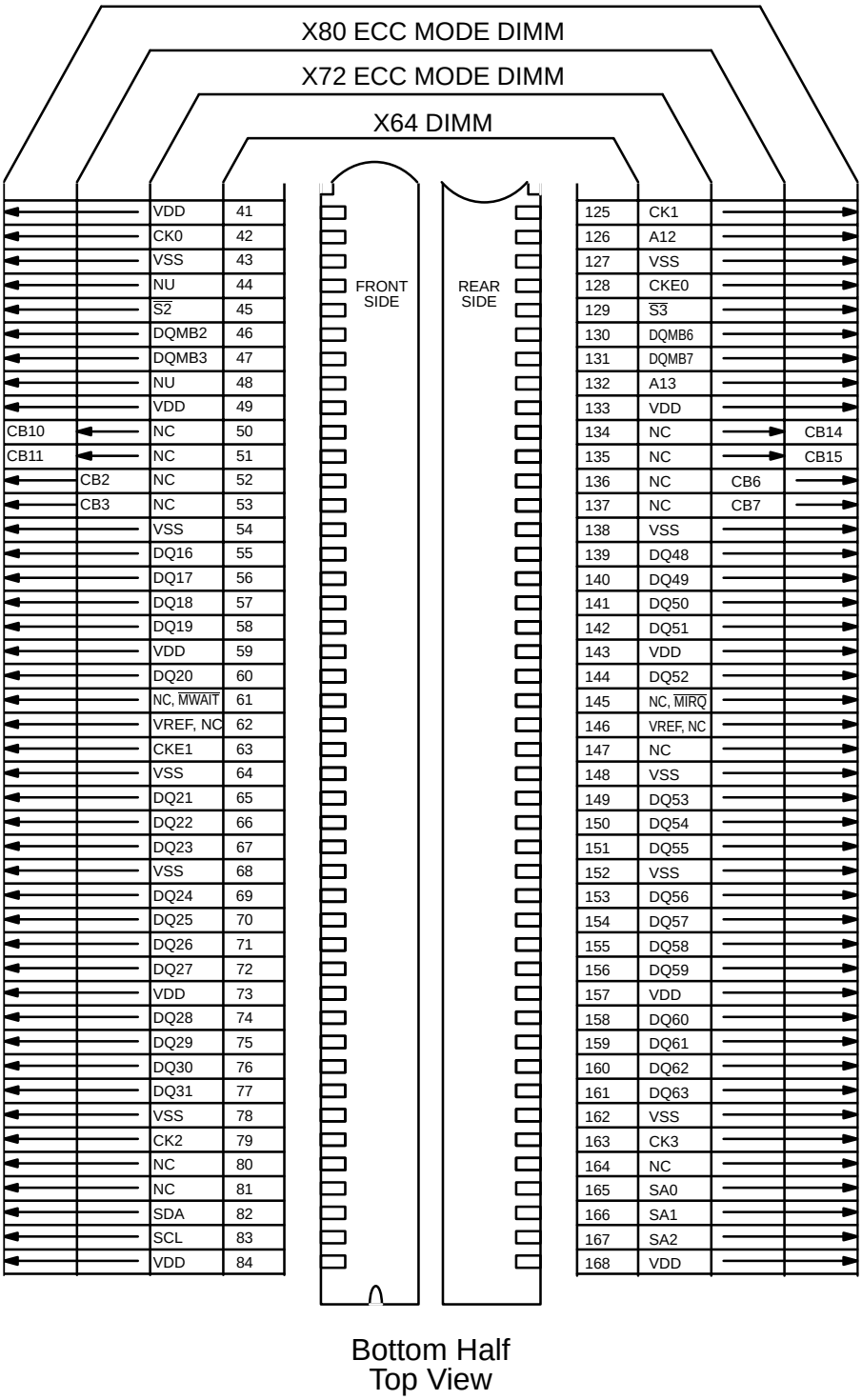


FIGURE 4.5.4–A

168 PIN, 64, 72, or 80 BIT SDRAM DIMM PINOUT, TOP HALF



Bottom Half
Top View

FIGURE 4.5.4–B
168 PIN, 64, 72, or 80 BIT SDRAM DIMM PINOUT, BOTTOM HALF

Module Configuration	SDRAM Organization	Option 1			Option 2			Option 3		
		# Bank addr.	$\overline{RAS}$ addr.	$\overline{CAS}$ addr.	# Bank addr.	$\overline{RAS}$ addr.	$\overline{CAS}$ addr.	# Bank addr.	$\overline{RAS}$ addr.	$\overline{CAS}$ addr.
1M x 64/72/80	1M x 16	1	11	8						
2M x 64/72/80	1M x 16	1	11	8						
2M x 64	2M x 32	2	11	8						
2M x 64/72/80	2M x 8	1	11	9						
3M x 64/72	2M x 8 1M X 16	1	11 11	9 8						
4M x 64/72/80	2M x 8	1	11	9						
4M x 64	2M x 32	2	11	8						
4M x 64/72/80	4M x 4	1	11	10						
4M x 64/72/80	4M x 16	2	12	8	1	13	8			
6M x 64	4M x 16 2M X 32	2	12 12	8 7	1	13 13	8 7			
8M x 64/72/80	4M x 16	2	12	8	1	13	8			
8M x 64	8M x 32	2	13	8	2	12	9			
8M x 64/72/80	8M x 8	2	12	9	1	13	9			
12M x 64/72	8M x 8 4M X 16	2	12 12	9 8	1	13 13	9 8			
16M x 64/72/80	8M x 8	2	12	9	1	13	9			
16M x 64	8M x 32	2	13	8	2	12	9			
16M x 64/72/80	16M x 4	2	12	10	1	13	10			
16M x 64/72/80	16M x 16	2	13	9						
24M x 64	16M x 16 8M X 32	2	13 13	9 8						
32M x 64/72/80	16M x 16	2	13	9						
32M x 64/72/80	32M x 8	2	13	10						
48M x 64/72	32M x 8 16M x 16	2	13 13	10 9						
64M x 64/72/80	32M x 8	2	13	10						
64M x 64/72/80	64M x 4	2	13	11						
(Note: All options possible with SDRAM standards are shown)										

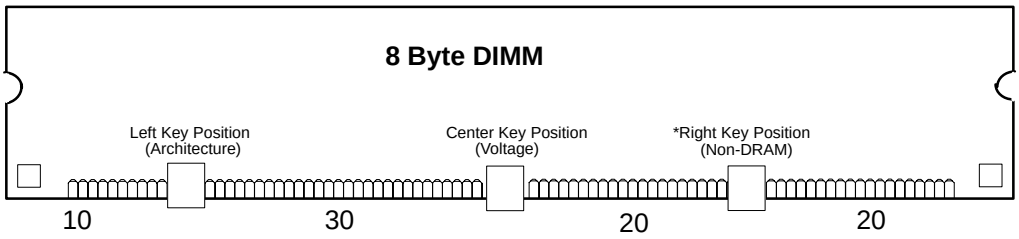
b. Allowable configurations: (Byte 11)
   - x64 (Non-parity, Byte controls)
   - x72 (ECC-optimized, Byte controls)
   - x80 (ECC-optimized, Byte controls)

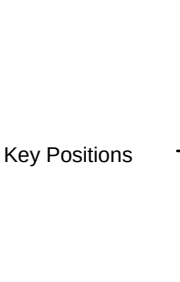
c. Functional Attributes:
   - Power Supply Voltage/Interface levels (Byte 8)
   - SDRAM cycle time (Byte 9)
   - SDRAM access from Clock (Byte 10)
   - Refresh rate/type (Byte 12)
   - SDRAM module attributes (Byte 13)
   - SDRAM device attributes (Bytes 14 - 20)
   - Primary/Secondary DRAM (Bytes 21 - 22)

Figure 4.5.4–C
168 Pin UNBUFFERED SDRAM DIMM SPD ASSIGNMENTS

Buffered	Unbufffered
All signals except RAS and Data are buffered	No buffers, all DRAM signals are connected directly to DIMM tab pins
11 Pins are used for DIMM attributes (PDE, PD1-8, ID0-1)	5 pins are used for DIMM attributes (SDA, SCL, SA0-2)
CAS Pin assignment sequence optimized for buffer placement 0, 1 2, 3 4, 5 6, 7	CAS Pin signals are re-assigned for optimal DRAM placement 0, 4 1, 5 2, 6 3, 7
ECC DIMMs use subset of CAS signals for word selection (CAS0/1 and CAS4/5)	All DIMM types use byte selection (CAS0-7)
Address 0 to the DRAMs is sourced from separate pins (A0, B0) for 4 byte interleave	Single address pin (A0)
Data pin assignment uses both X64/X72 and X80 numbering schemes	Data pin assignment is changed to single x80 numbering scheme with x64 and x72 as subsets
Non-Parity is subset of Parity with inter-mixed Parity bits unconnected (PQ8, 17, 26, 35, 44, 53, 62, 71)	All DIMM types use the same sequential 64 data pins (DQ0-63). Eight center pins (CB0-7) are used as Parity/Check Bits for x72 Parity/ECC DIMMs. An additional 8 center pins (CB8-15) are used for the x80 ECC DIMMs.
32 Power/Gnd Pins VCC - 16 VSS - 16	35 Power/Gnd Pins VCC - 17 (1 additional pin) VSS - 18 (2 additional pins)
Unused Pins - 18	Unused Pins - 14
Left Key Definition SDRAM STD DRAM RFU	Left Key Definition modified RFU Buffered Assembly (DRAM/SDRAM) Unbuffered Assembly (DRAM/SDRAM)

FIGURE 4.5.4–D
Comparison of 168 Pin Buffered & Unbuffered DRAM & SDRAM DIMM





Left Key Position	Center Key	*Right Key
RFU	5V	No Key
**1st GENERATION 168 PIN DIMM	3.3V	No Key
***2nd GENERATION 168 PIN DIMM	X.XV	No Key

* For DRAM/SDRAM assemblies, this area is poplulated with pads.
**1st Generation: Initial 168P DIMM standard described in Sec. 4.5.1. This standard included buffering on all inputs except RAS and DQs as well as Parallel Presence Detect (PD).
*** 2nd Generation: Originally described as “Unbuffered” DRAM & SDRAM. DIMMs, these DIMMs have Serial PDs, and both DRAM & SDRAM versions.

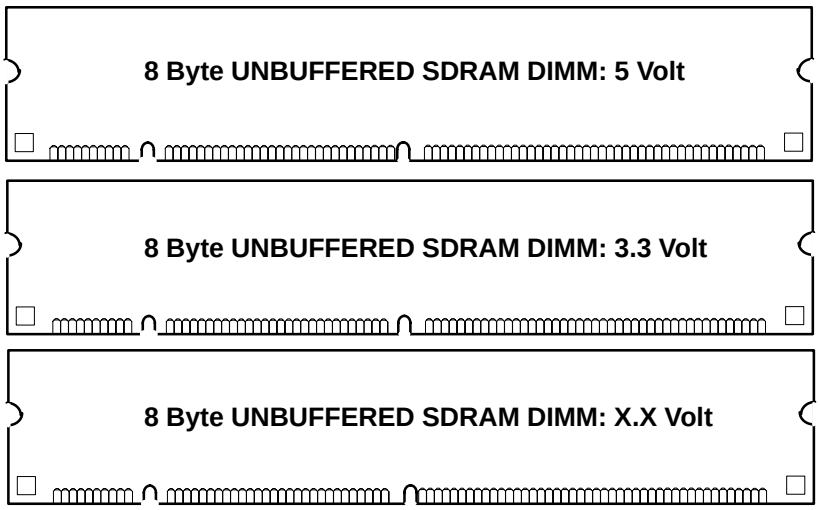


FIGURE 4.5.4–E
168 Pin SDRAM DIMM Keying Methodology

Pin #	DRAM DIMM	SDRAM DIMM
28	$\overline{CAS0}$	DQMB0
29	$\overline{CAS1}$	DQMB1
30	$\overline{RAS0}$	S0
31	$\overline{OE}0$	NU
39	A12	BA1
42	NU	CK0
44	$\overline{OE}2$	NU
45	$\overline{RAS}2$	$\overline{S}2$
46	$\overline{CAS}2$	DQMB2
47	$\overline{CAS}3$	DQMB3
48	$\overline{WE}2$	NU
62	NU	V_{REF} (IF APPLICABLE)
63	NC	CKE1
79	NU	CK2
111	NU	$\overline{CAS}$
112	$\overline{CAS}4$	DQMB4
113	$\overline{CAS}5$	DQMB5
114	$\overline{RAS}1$	$\overline{S}1$
115	NU	$\overline{RAS}$
122	A11	BA0
123	A13	A11
125	NU	CK1
126	NU	A12
128	NU	CKE0
129	$\overline{RAS}3$	$\overline{S}3$
130	$\overline{CAS}6$	DQMB6
131	$\overline{CAS}7$	DQMB7
132	NU	A13
146	NU	V_{REF} (IF APPLICABLE)
163	NC	CK3

Notes:
1. A10 on DRAM DIMM is also AP on SDRAM DIMM
2. A11 on DRAM DIMM is also BS0 on SDRAM DIMM
3. A12 on DRAM DIMM is also BS1 on SDRAM DIMM (for 4 Bank SDRAMs)

FIGURE 4.5.3–F
Pinout Comparison, 168 Pin DRAM & SDRAM DIMM

X 64 (Non–parity)						
			CLK Loading			
SDRAM Data Width	# of Banks on DIMM	Total # SDRAMs	CK0	CK1	CK2	CK3
X4	1	16	4	4	4	4
X8	1	8	4	4	*	*
X8/X16	2	12	*2–4	*2–4	*2–4	*2–4
X16	1	4	4	*	*	*
X32	1	2	*2	*	*	*
X8	2	16	4	4	4	4
X16	2	8	4	4	*	*
X16/X32	2	6	*2–4	*2–4	*	*
X32	2	4	4	*	*	*

X 72 (ECC)						
			CLK Loading			
SDRAM Data Width	# of Banks on DIMM	Total # SDRAMs	CK0	CK1	CK2	CK3
X4	1	18	** 4 or 5	** 4 or 5	** 4 or 5	** 4 or 5
X8	1	9	** 4 or 5	** 4 or 5	*	*
X8/X16	2	14	*3–4	*3–4	*3–4	*3–4
X16/X4	1	6	4 (MAX)	4 (MAX)	*	*
X32/X8	1	3	*3	*	*	*
X8	2	18	** 4 or 5	** 4 or 5	** 4 or 5	** 4 or 5
X16/X4	2	12	4	4	4	
X32/X8	2	6	4 (MAX)	4 (MAX)	*	*

X 80 (ECC)						
			CLK Loading			
SDRAM Data Width	# of Banks on DIMM	Total # SDRAMs	CK0	CK1	CK2	CK3
X4	1	20	5	5	5	5
X8	1	10	5	5	*	*
X16	1	5	5	*	*	*
X32/X8	1	4	4	*	*	*
X8	2	20	5	5	5	5
X16	2	10	5	5	*	*
X32/X8	2	8	4	4	*	*

Notes:

* add padding capacitance per clock wiring detail.

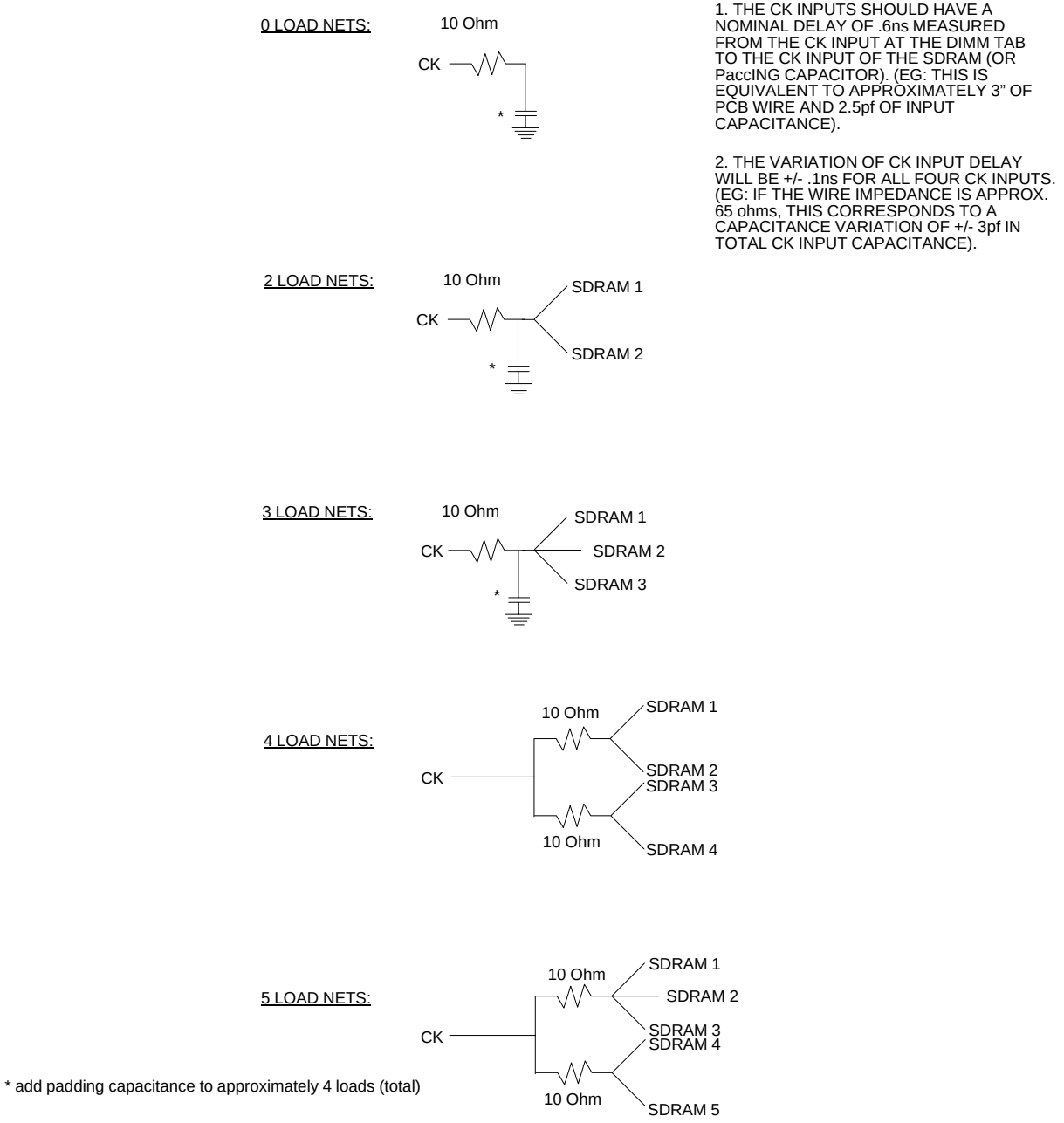
** CK0 + CK2 must total 9 SDRAMs, CK1 + CK3 must total 9 SDRAMs (to allow clock “dotting” at system).

Figure 4.5.4–G
168 Pin UNBUFFERED SDRAM DIMM CLOCK LOADING

TARGET CLOCK (CK) SPECIFICATION:

1. THE CK INPUTS SHOULD HAVE A NOMINAL DELAY OF .6ns MEASURED FROM THE CK INPUT AT THE DIMM TAB TO THE CK INPUT OF THE SDRAM (OR PaccING CAPACITOR). (EG: THIS IS EQUIVALENT TO APPROXIMATELY 3" OF PCB WIRE AND 2.5pf OF INPUT CAPACITANCE).

2. THE VARIATION OF CK INPUT DELAY WILL BE +/- .1ns FOR ALL FOUR CK INPUTS. (EG: IF THE WIRE IMPEDANCE IS APPROX. 65 ohms, THIS CORRESPONDS TO A CAPACITANCE VARIATION OF +/- 3pf IN TOTAL CK INPUT CAPACITANCE).



* add padding capacitance to approximately 4 loads (total)

Figure 4.5.4–H
168 Pin UNBUFFERED DRAM DIMM CLOCK WIRING

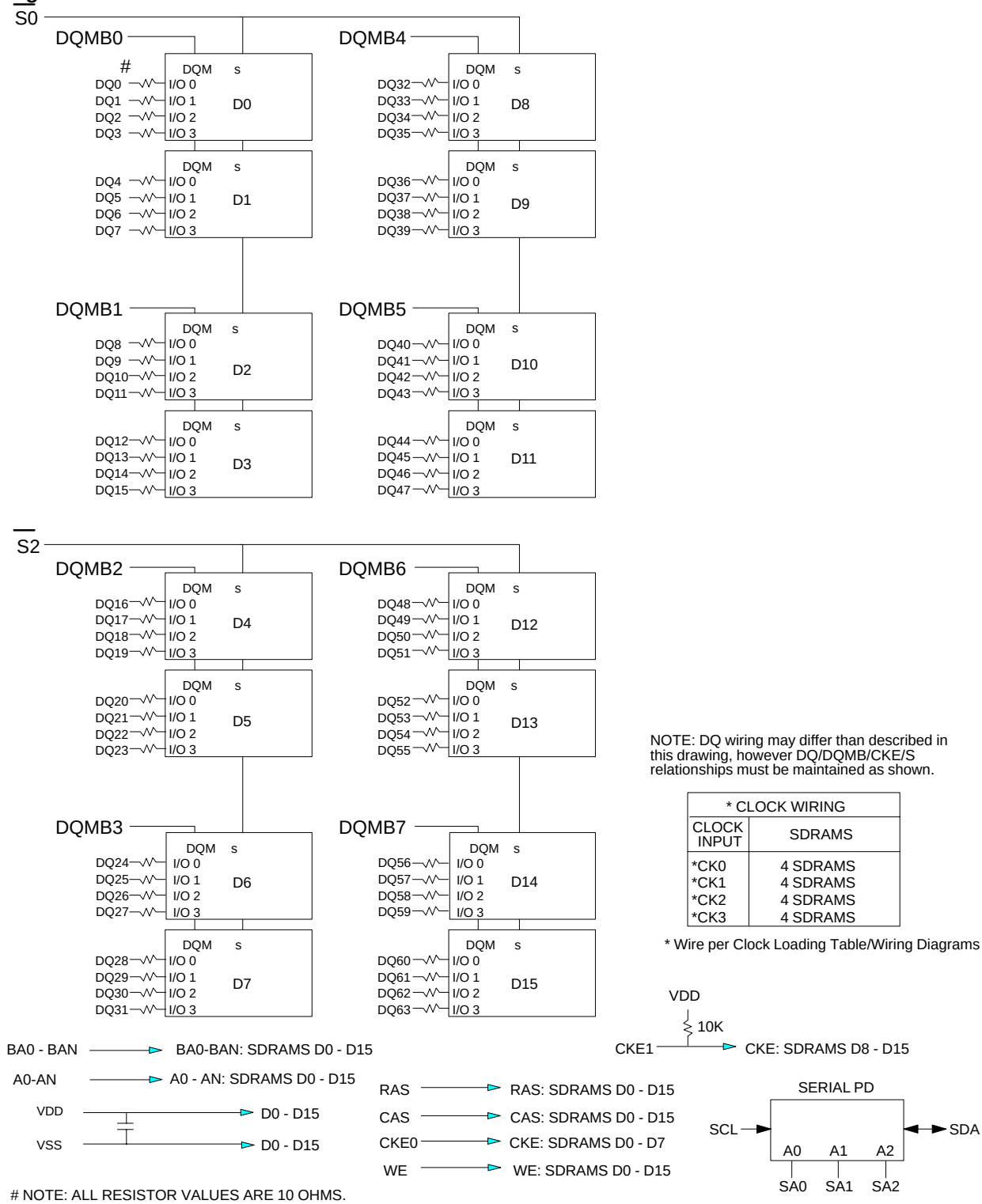


Figure 4.5.4–I
X64 SDRAM DIMM, 1 Bank with X4 SDRAMs

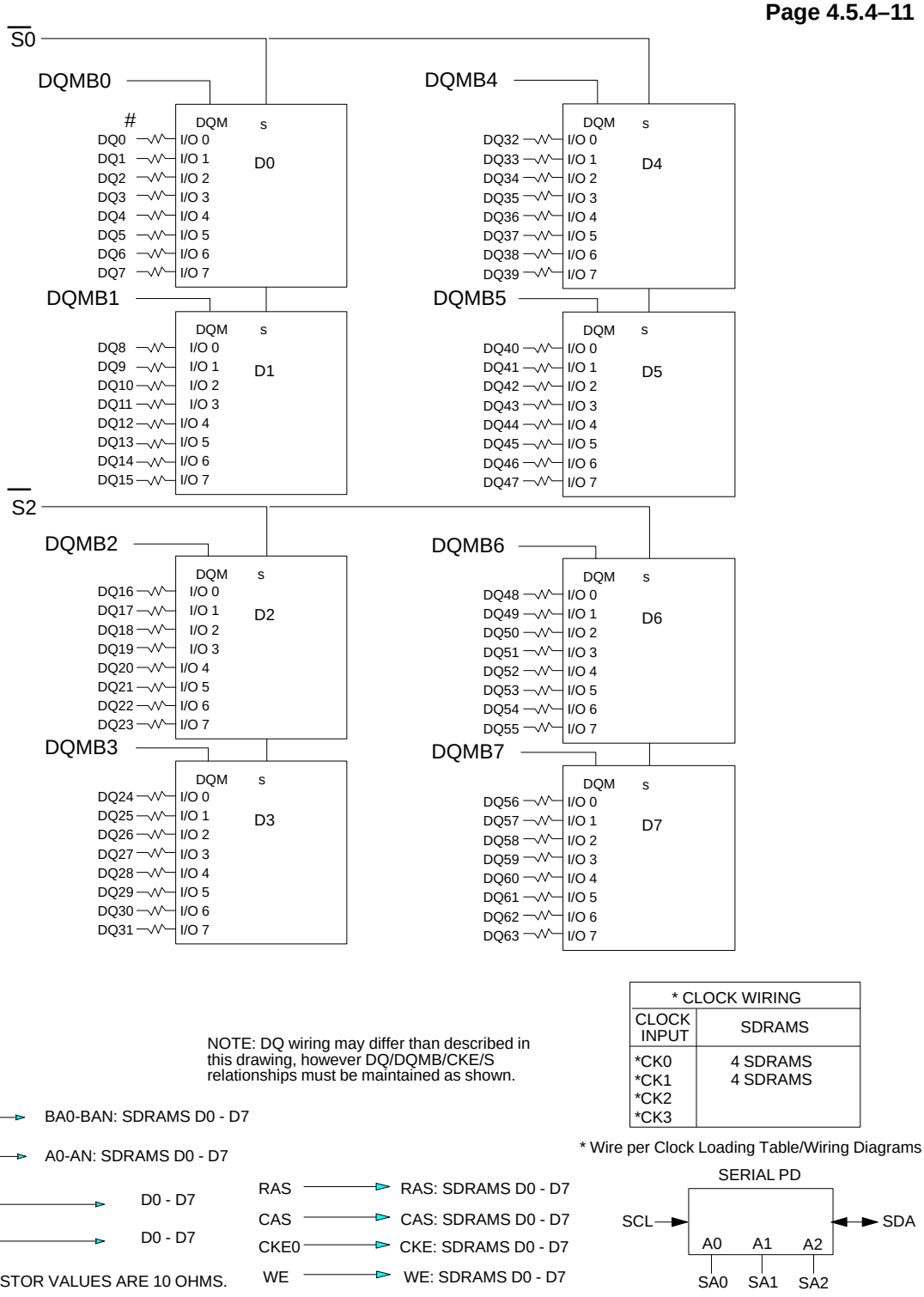
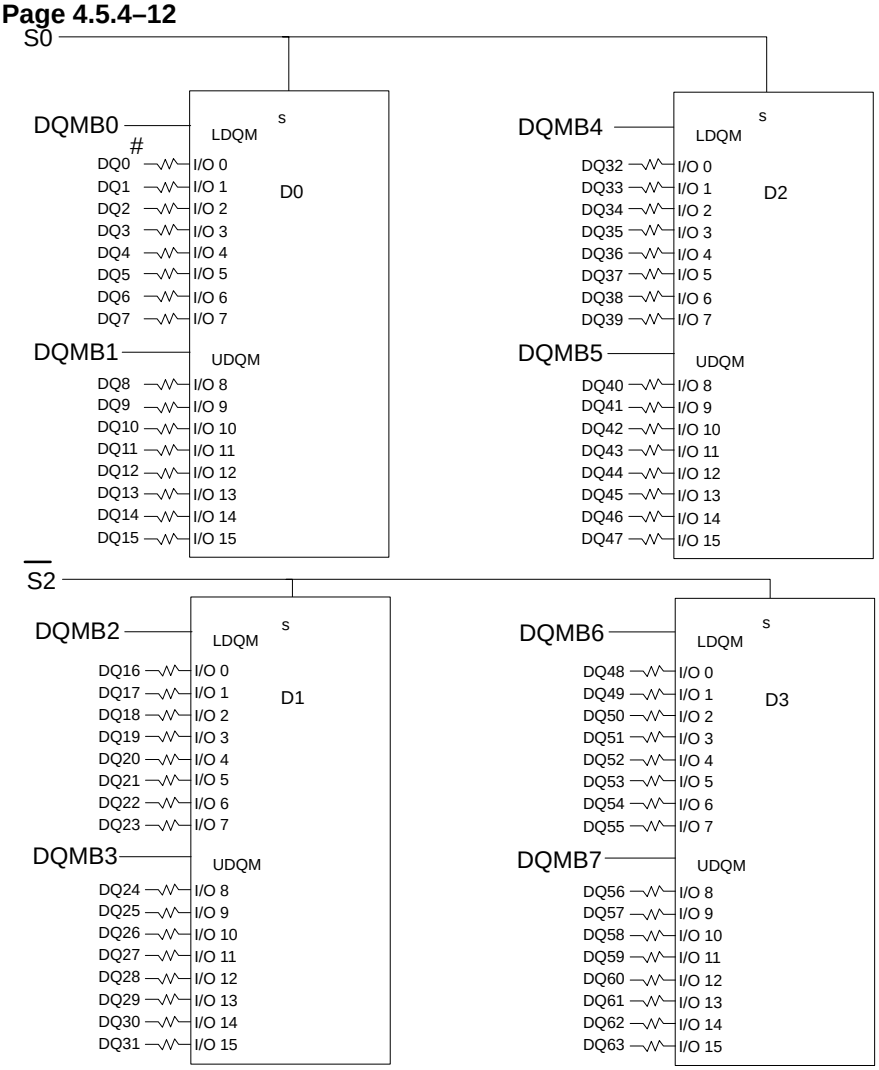
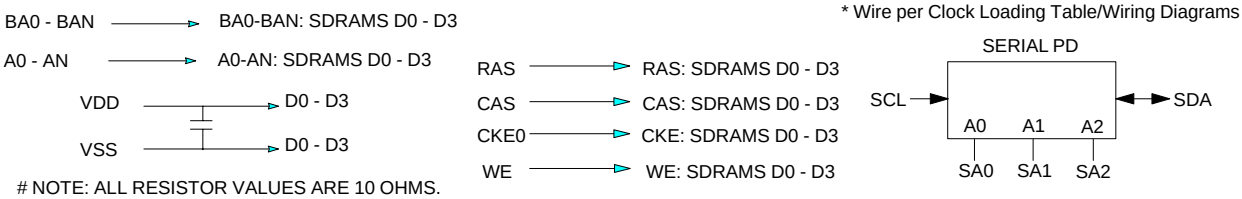


Figure 4.5.4–J
X64 SDRAM DIMM, 1 Bank with X8 SDRAMs



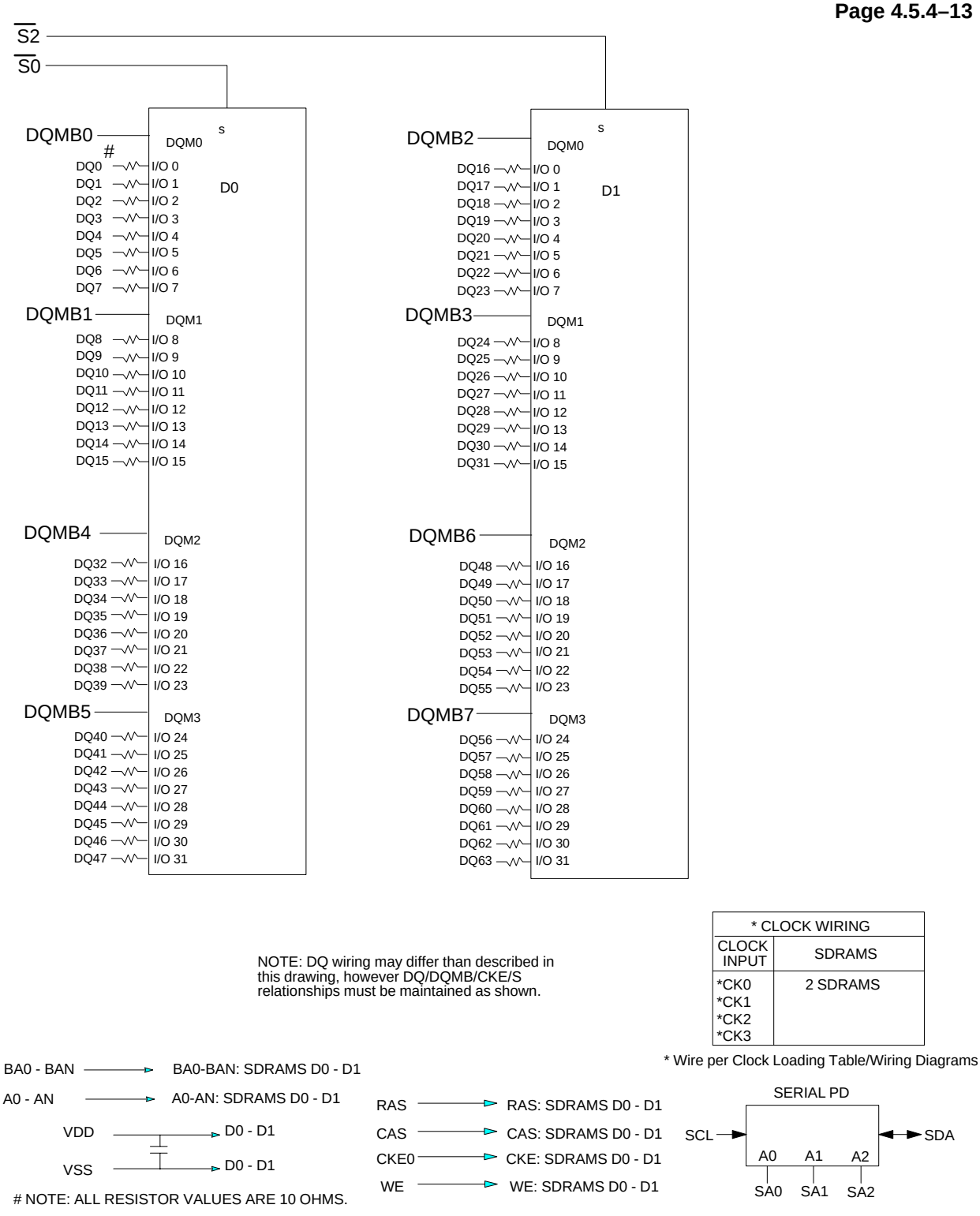
NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1 *CK2 *CK3	4 SDRAMS



NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–K
X64 SDRAM DIMM, 1 Bank with X16 SDRAMs



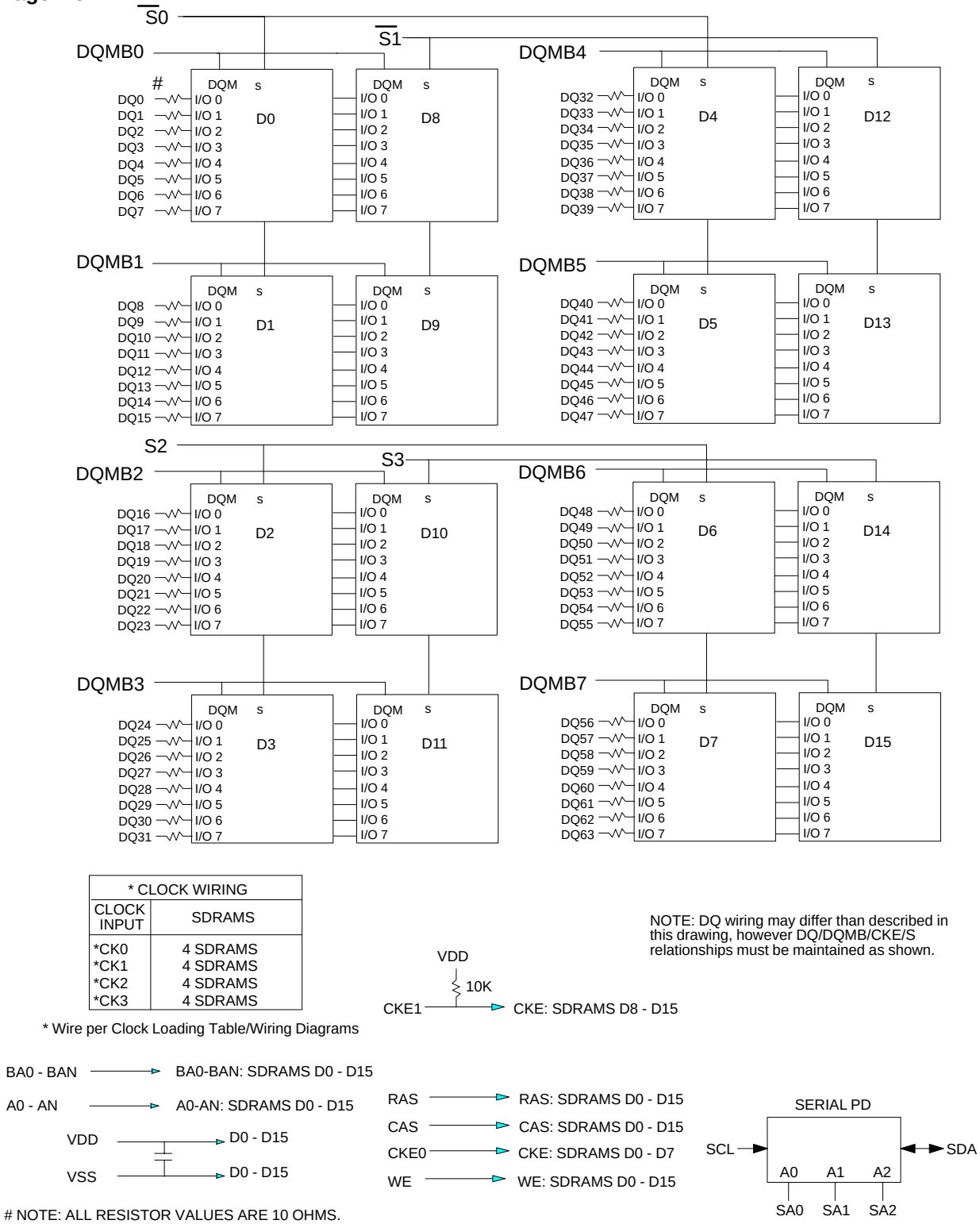
NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1 *CK2 *CK3	2 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–L
X64 SDRAM DIMM, 1 Bank with X32 SDRAMs



* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS
*CK2	4 SDRAMS
*CK3	4 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

VDD
10K
CKE1 → CKE: SDRAMS D8 - D15

BA0 - BAN → BA0-BAN: SDRAMS D0 - D15

A0 - AN → A0-AN: SDRAMS D0 - D15

VDD → D0 - D15

VSS → D0 - D15

RAS → RAS: SDRAMS D0 - D15

CAS → CAS: SDRAMS D0 - D15

CKE0 → CKE: SDRAMS D0 - D7

WE → WE: SDRAMS D0 - D15

SERIAL PD
SCL ↔ SDA
A0 A1 A2
SA0 SA1 SA2

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–M
X64 SDRAM DIMM, 2 Banks with X8 SDRAMs

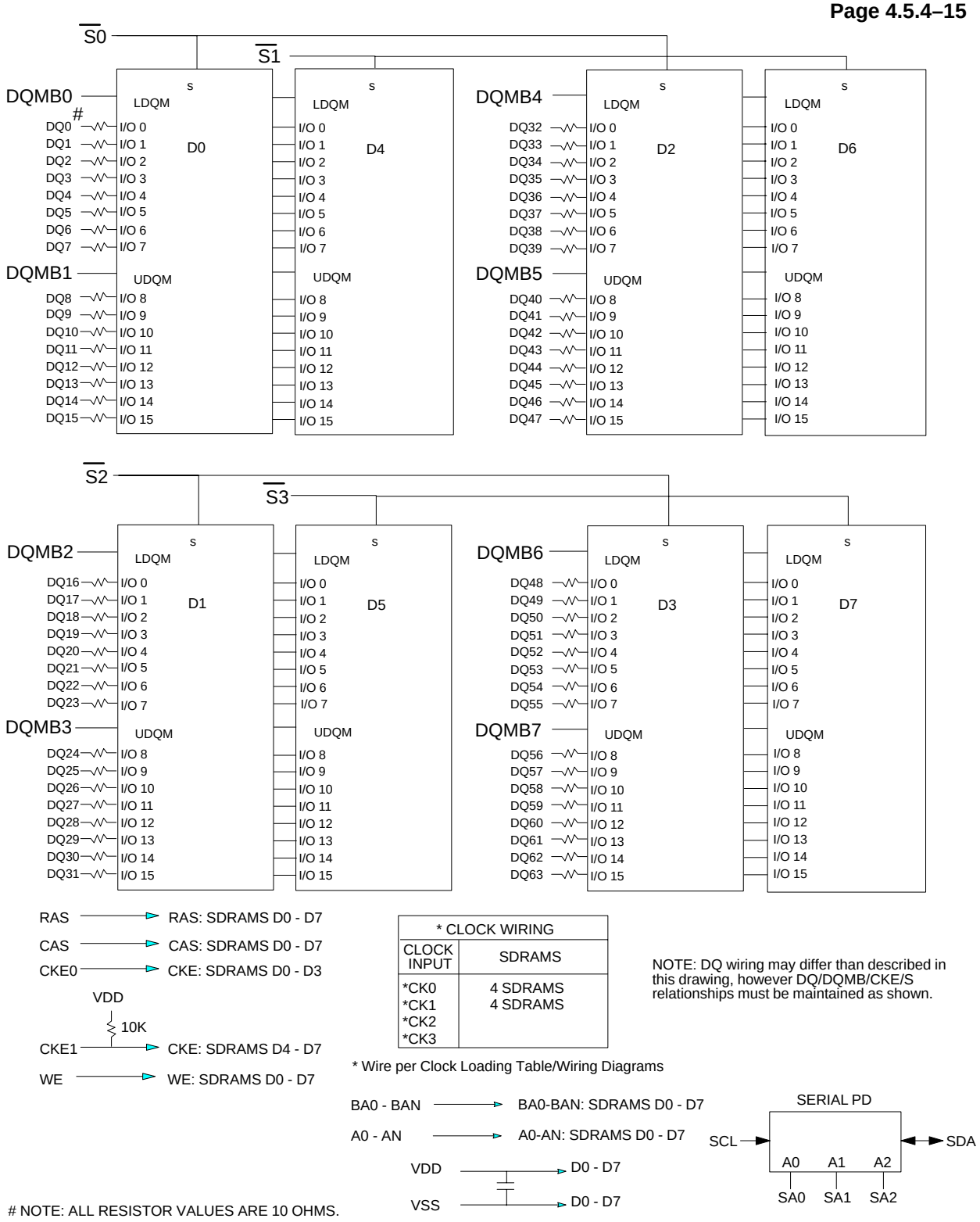


Figure 4.5.4–N
X64 SDRAM DIMM, 2 Banks with X16 SDRAMs

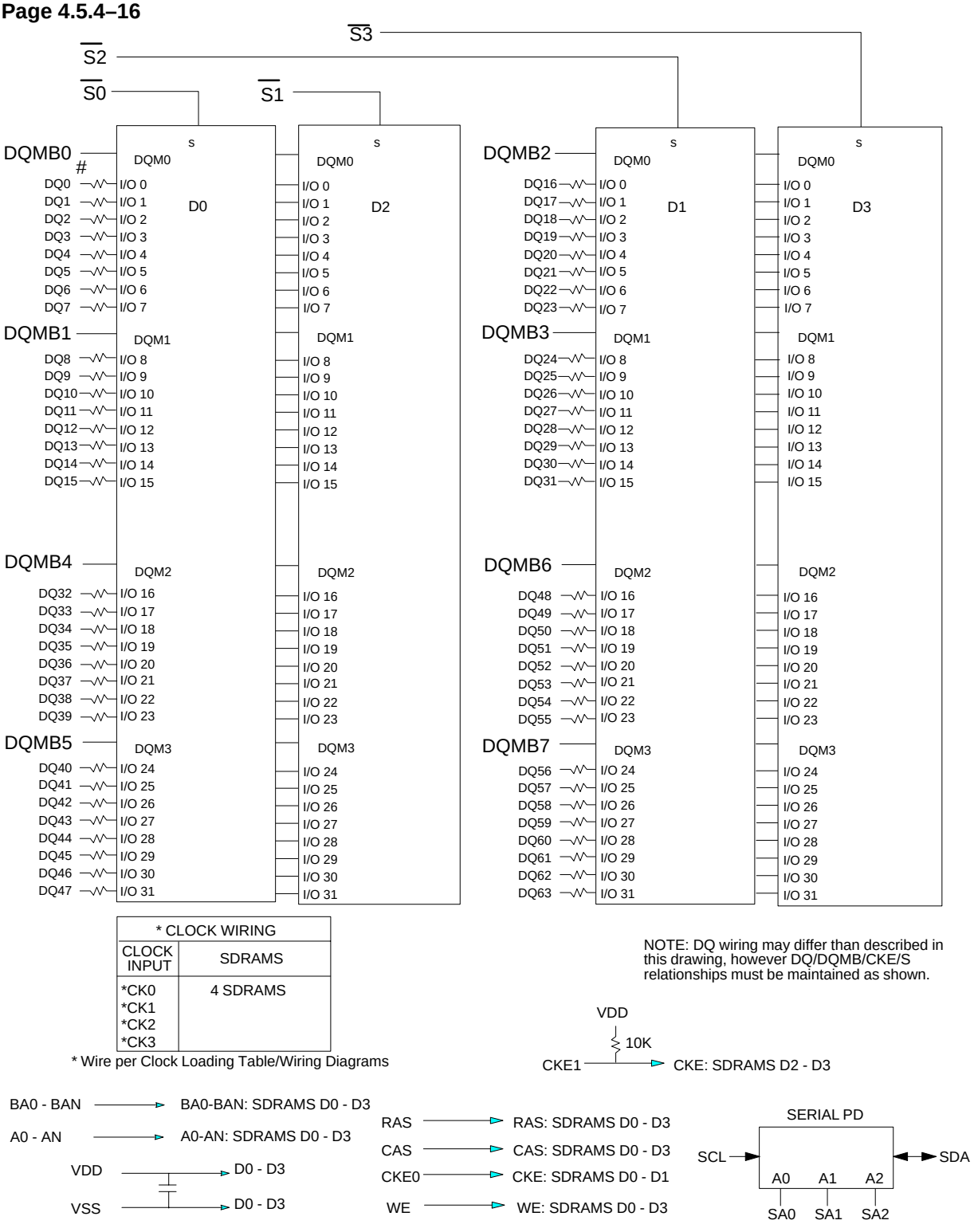
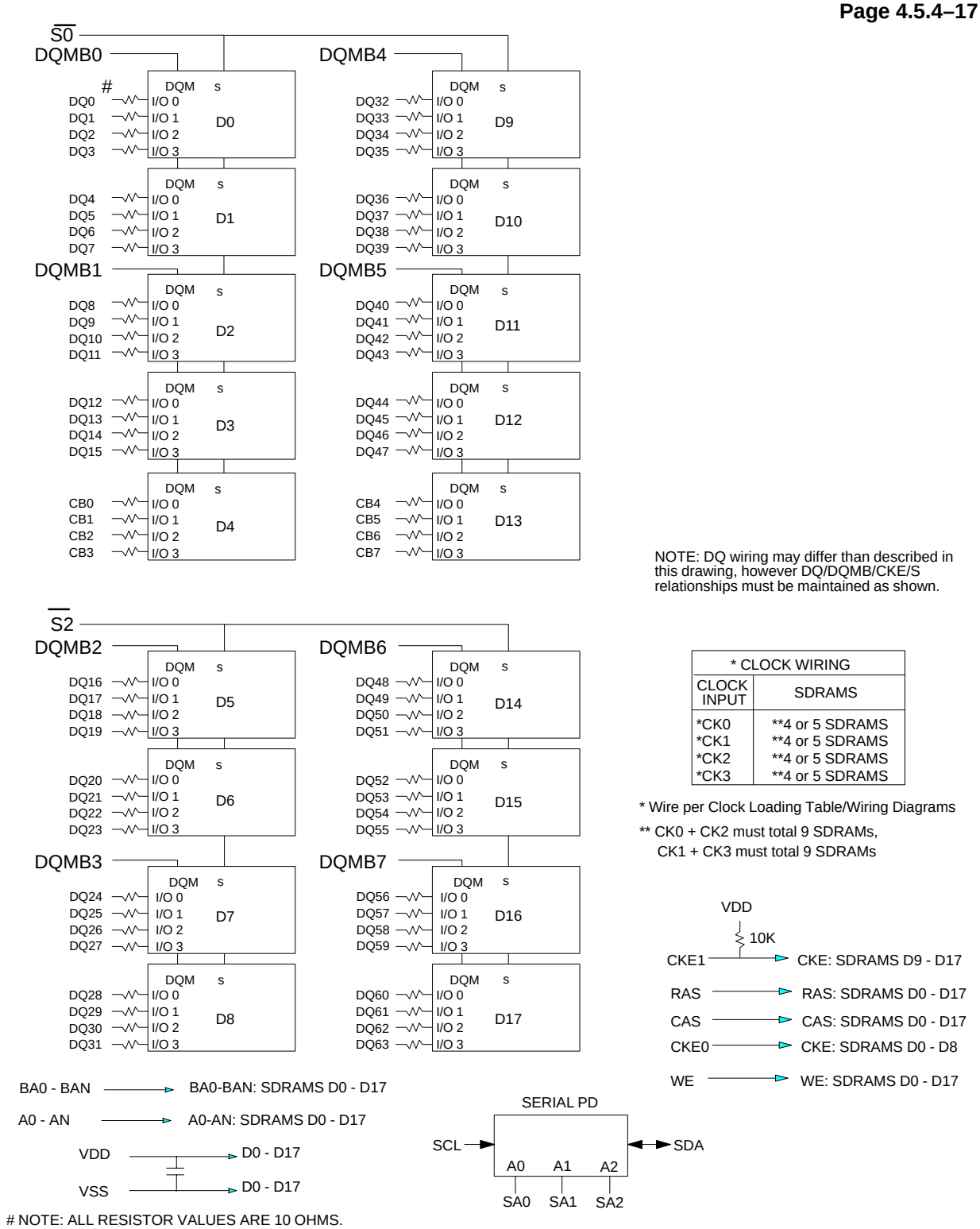


Figure 4.5.4–O
X64 SDRAM DIMM, 2 Banks with X32 SDRAMs



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

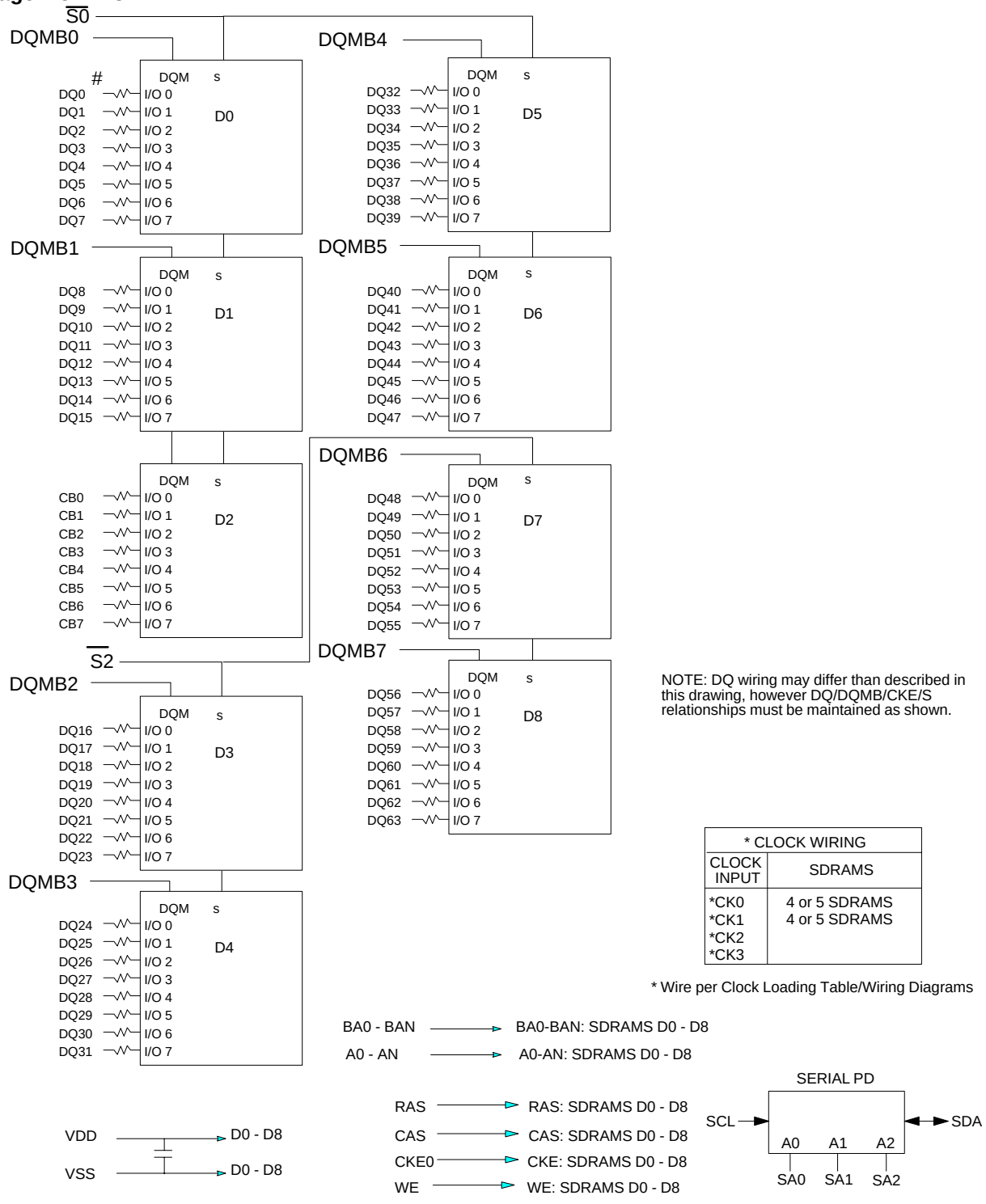
* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	**4 or 5 SDRAMS
*CK1	**4 or 5 SDRAMS
*CK2	**4 or 5 SDRAMS
*CK3	**4 or 5 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

** CK0 + CK2 must total 9 SDRAMs,
CK1 + CK3 must total 9 SDRAMs

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–P
X72 ECC SDRAM DIMM, 1 Banks with X4 SDRAMs



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	4 or 5 SDRAMS
*CK1	4 or 5 SDRAMS
*CK2	
*CK3	

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–Q
X72 ECC SDRAM DIMM, 1 Banks with X8 SDRAMs

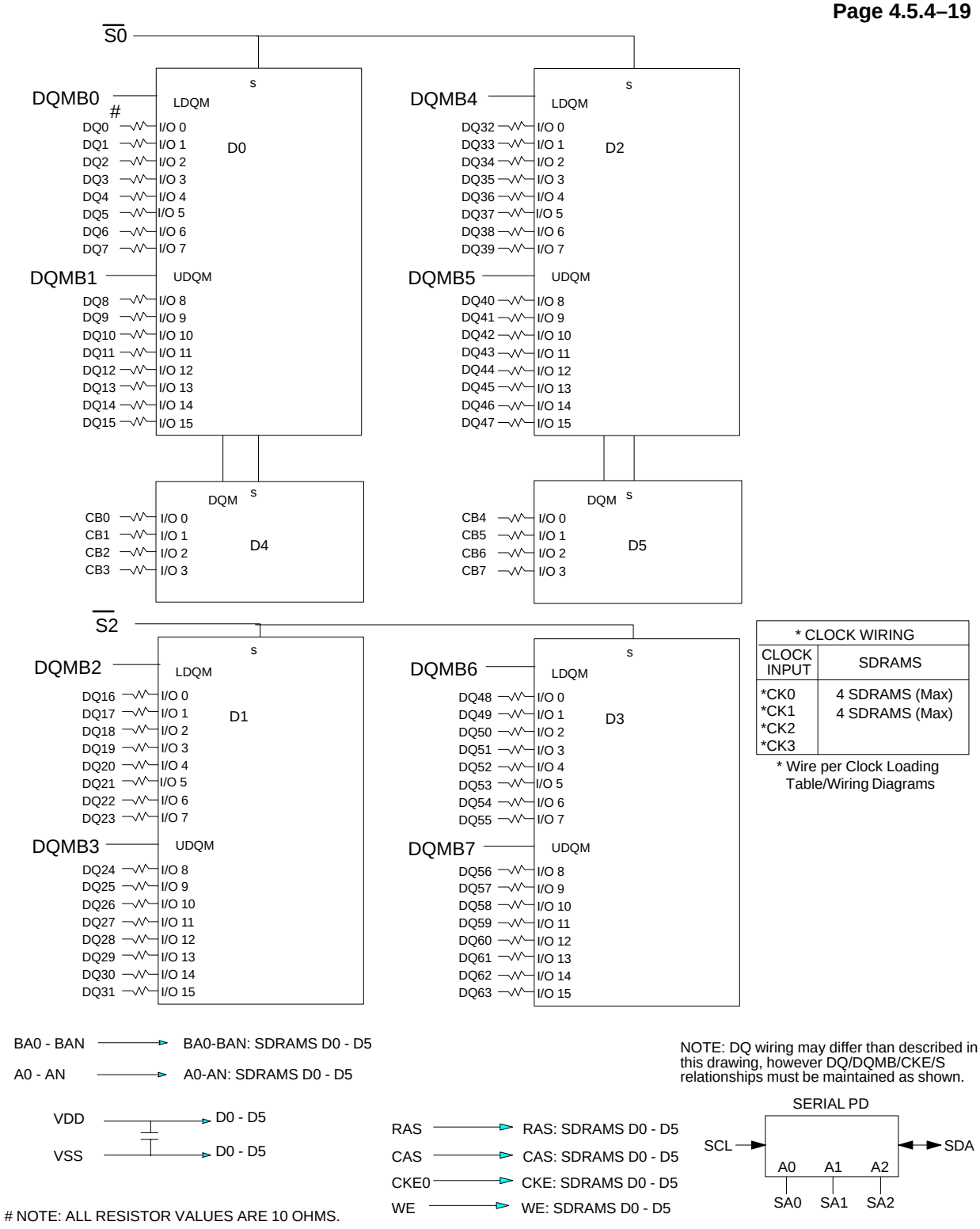
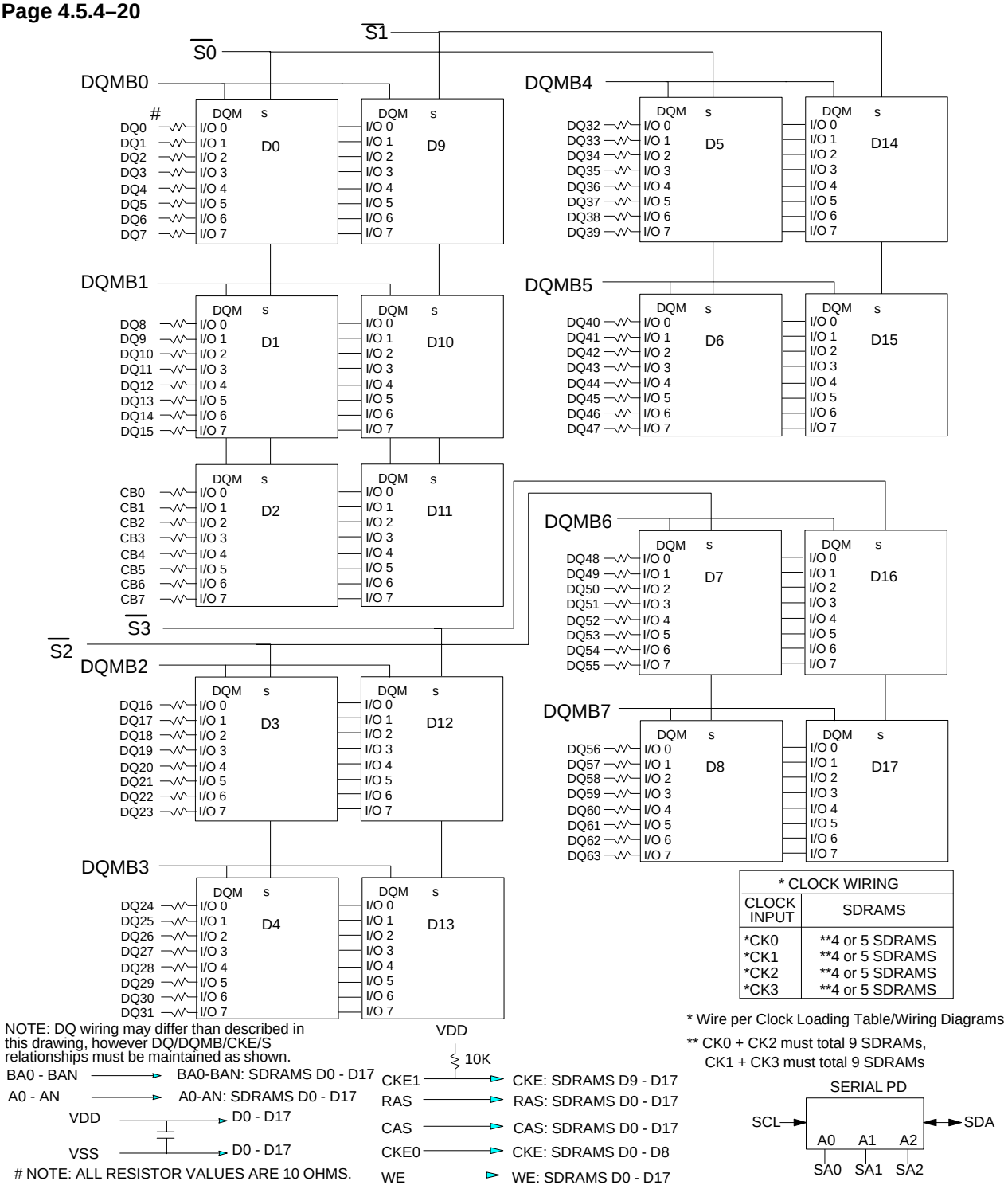
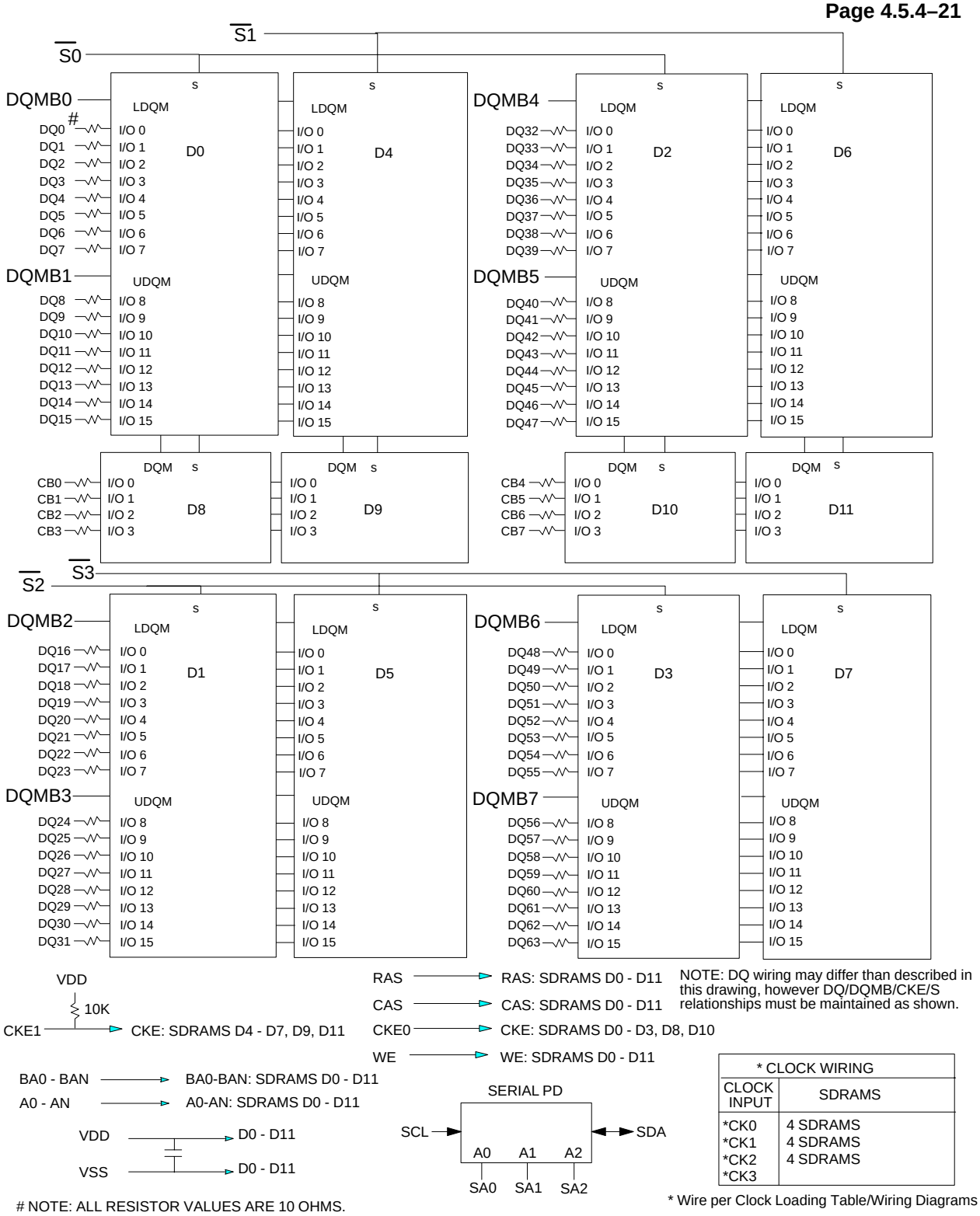


Figure 4.5.4–R
X72 ECC SDRAM DIMM, 1 Bank with X16 & X4 SDRAMs



NOTE: All future designs using this configuration should use Version 2, which reduces the DQMB1 loading from 4 to 3 SDRAMs. See Fig. 4.5.4–AC on P. 4.5.4–30

Figure 4.5.4–S
X72 ECC SDRAM DIMM, 2 Banks with X8 SDRAMs



* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS
*CK2	4 SDRAMS
*CK3	

* Wire per Clock Loading Table/Wiring Diagrams

Figure 4.5.4–T
X72 ECC SDRAM DIMM, 2 Banks with X16 & X4 SDRAMs

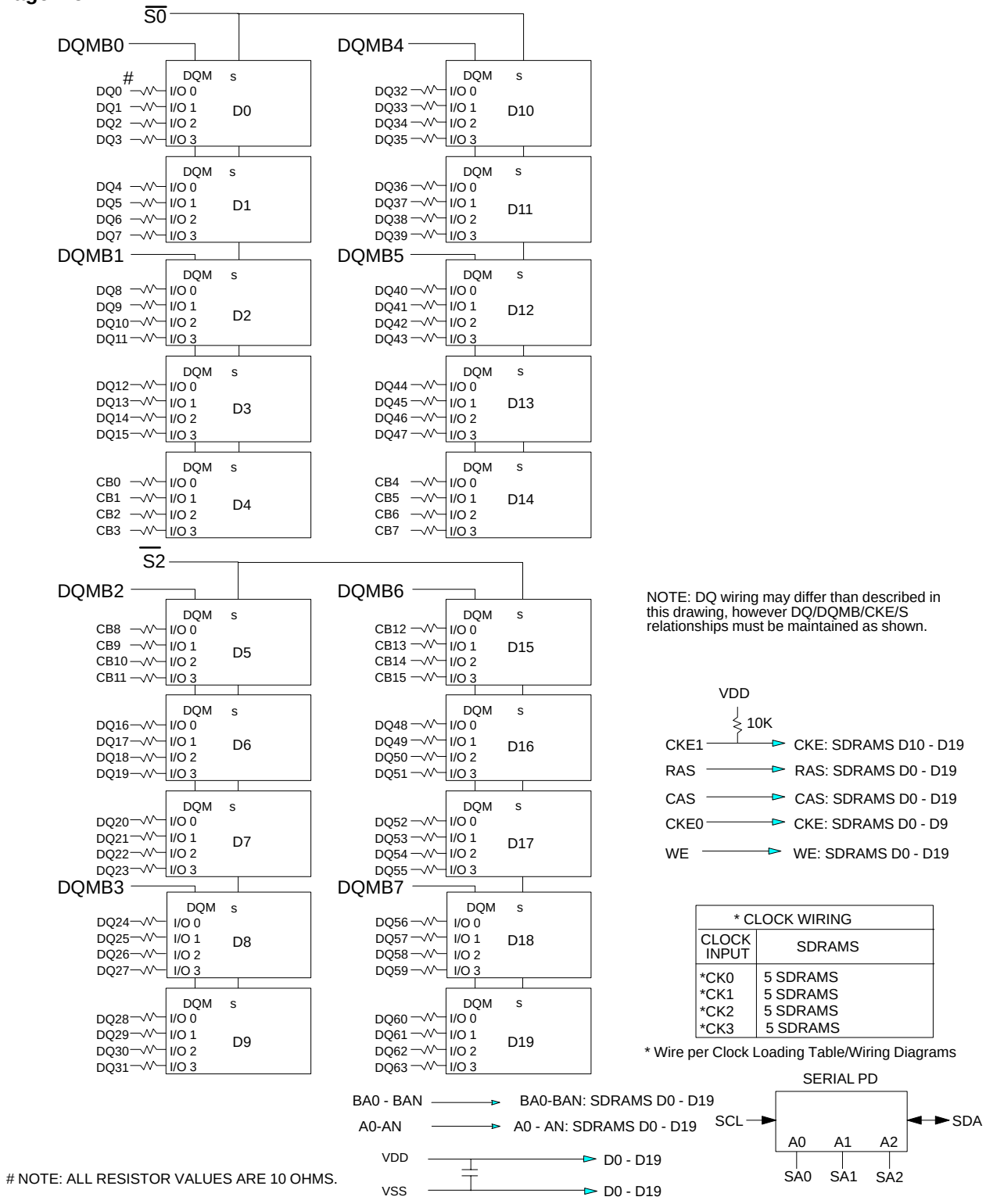
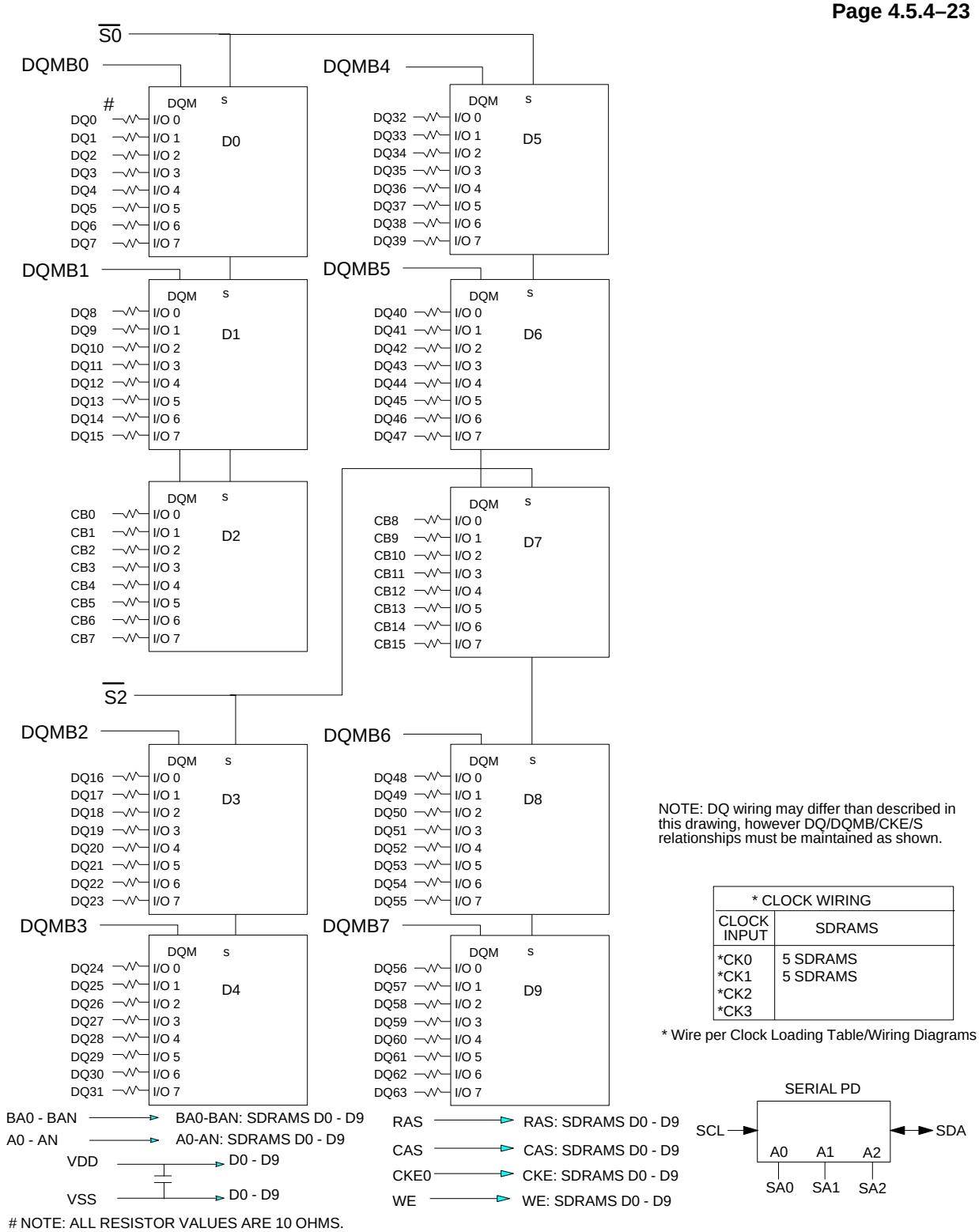


Figure 4.5.4–U
X80 SDRAM DIMM, 1 Bank with X4 SDRAMs



NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	5 SDRAMS
*CK1	5 SDRAMS
*CK2	
*CK3	

* Wire per Clock Loading Table/Wiring Diagrams

Figure 4.5.4–V
X80 ECC SDRAM DIMM, 1 Bank with X8 SDRAMs

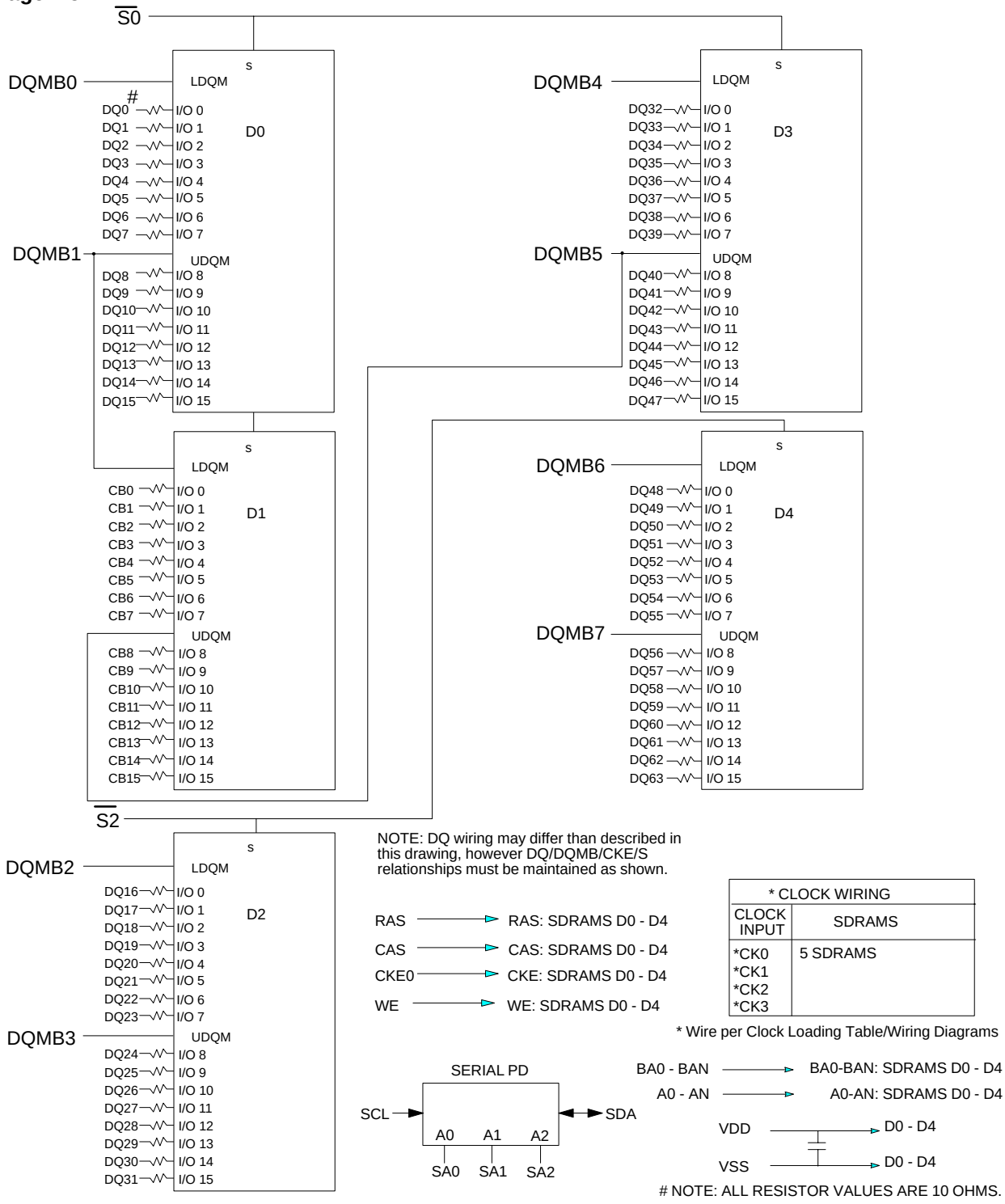
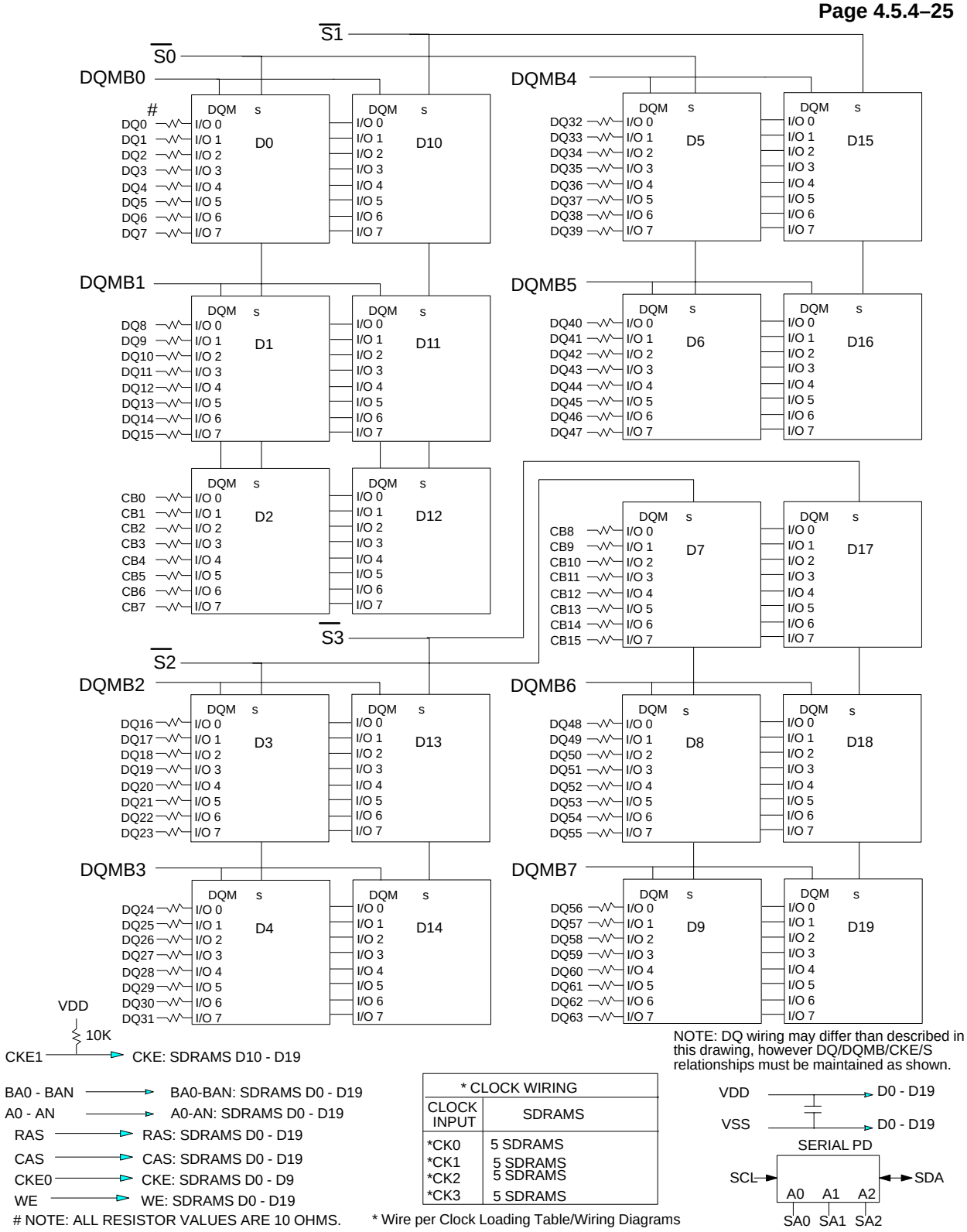


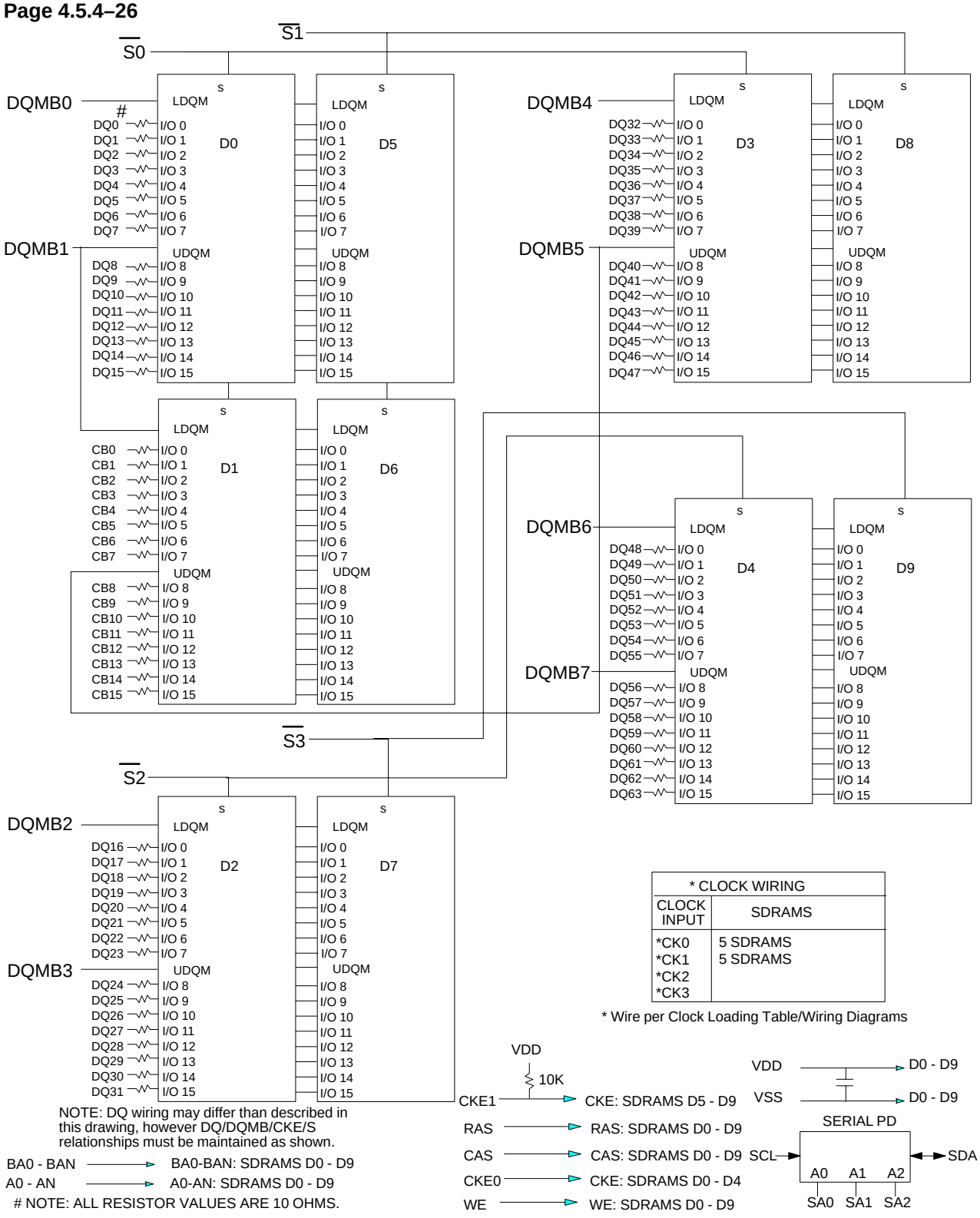
Figure 4.5.4–W
X80 ECC SDRAM DIMM, 1 Bank with X16 SDRAMs



* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	5 SDRAMS
*CK1	5 SDRAMS
*CK2	5 SDRAMS
*CK3	5 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

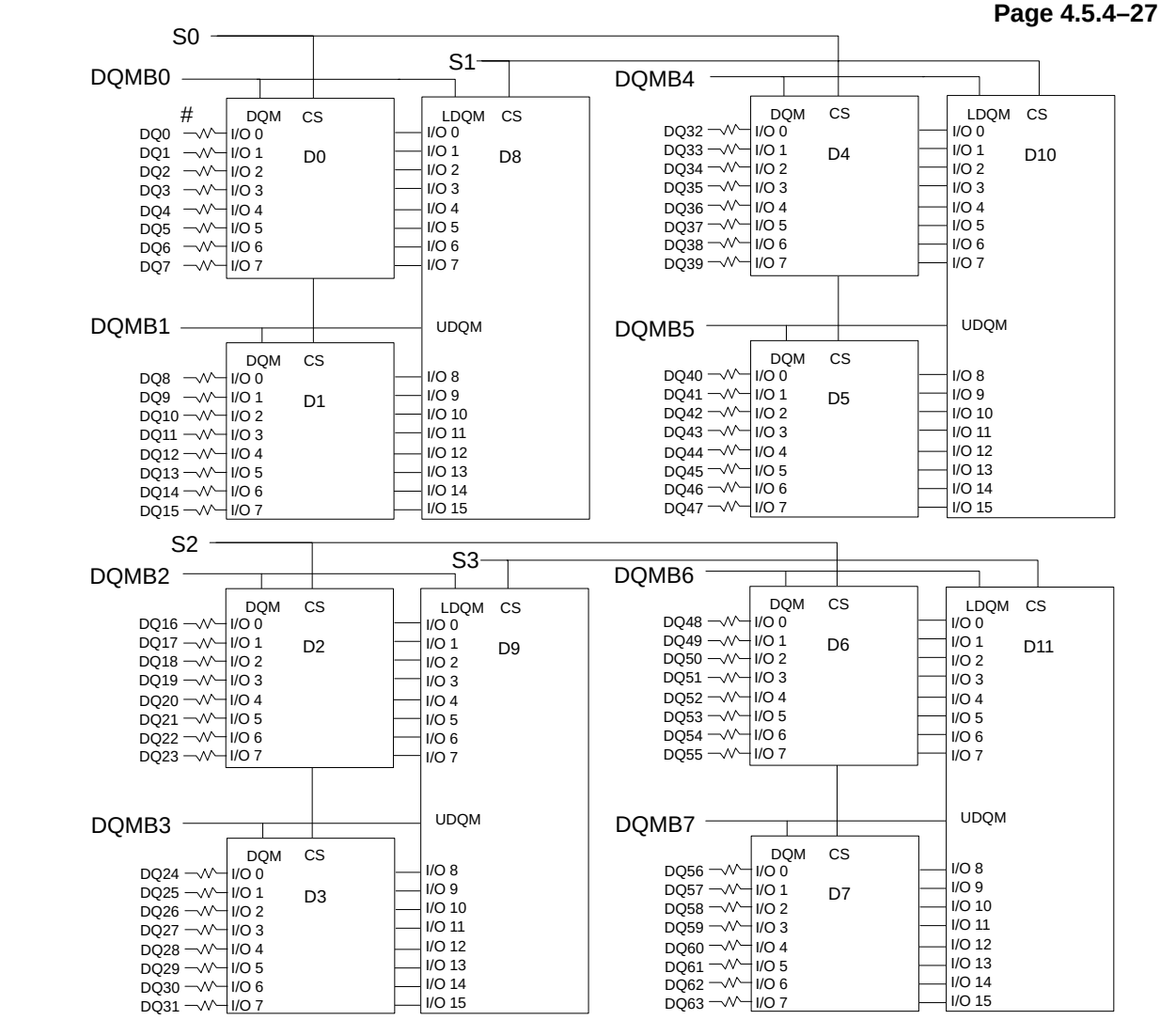
Figure 4.5.4–X
X80 ECC SDRAM DIMM, 2 Banks with X8 SDRAMs



* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	5 SDRAMS
*CK1	5 SDRAMS
*CK2	
*CK3	

* Wire per Clock Loading Table/Wiring Diagrams

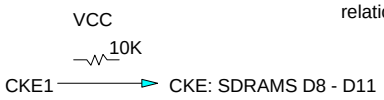
Figure 4.5.4–Y
X80 ECC SDRAM DIMM, 2 Banks with X16 SDRAMs

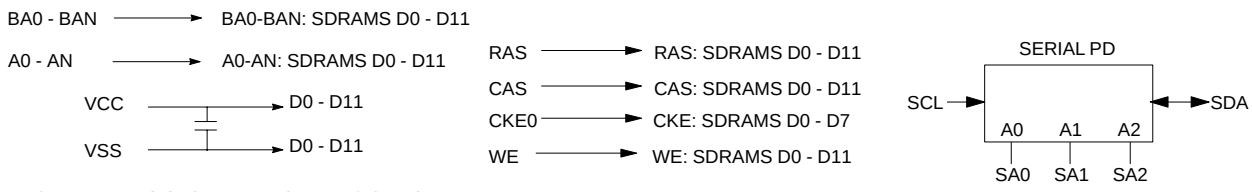


* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	2-4 SDRAMS
*CK1	2-4 SDRAMS
*CK2	2-4 SDRAMS
*CK3	2-4 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

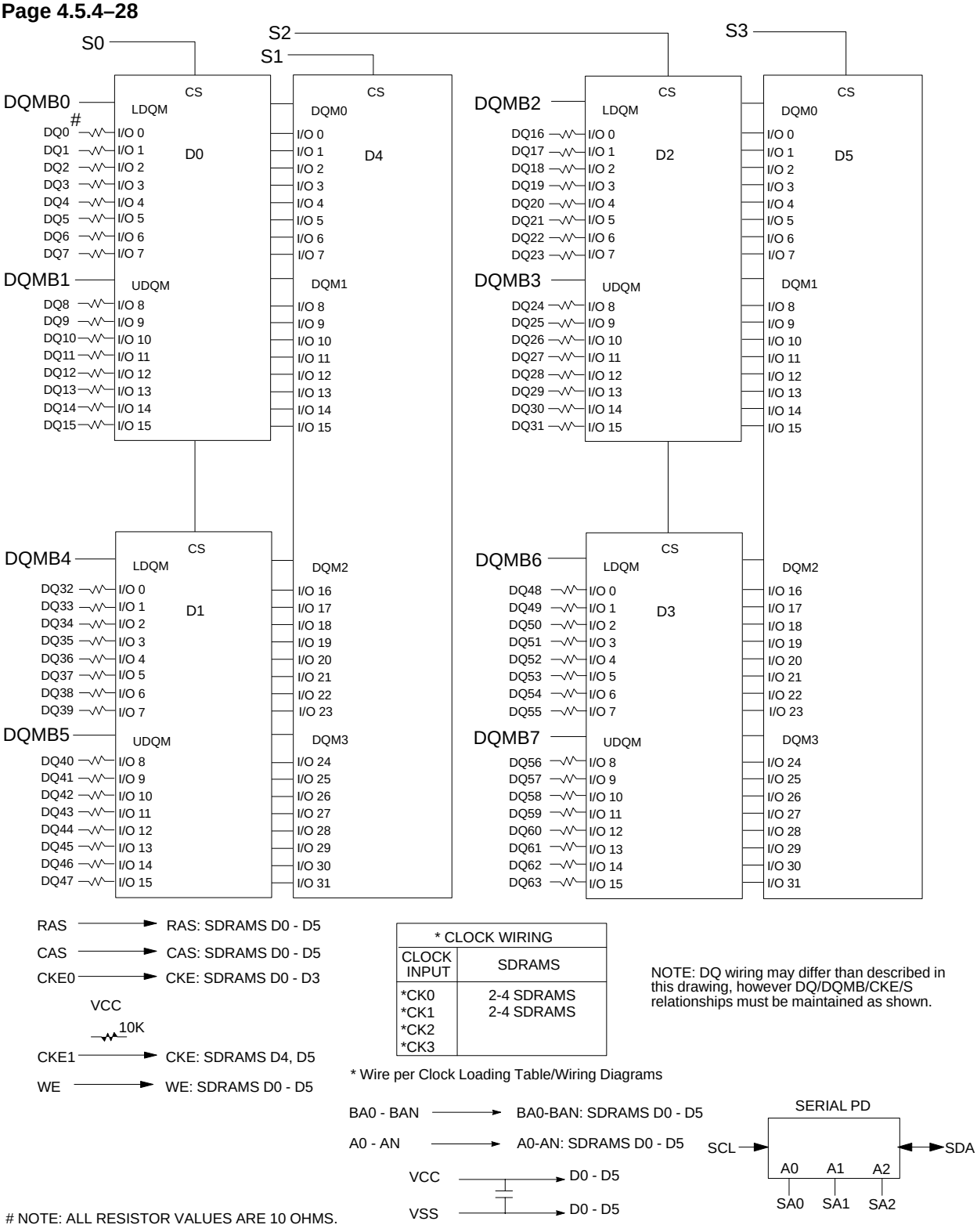
NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.





NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–Z
X64 SDRAM DIMM, 2 Banks with X8 & X16 SDRAMs



* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	2-4 SDRAMS
*CK1	2-4 SDRAMS
*CK2	
*CK3	

NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–AA
X64 SDRAM DIMM, 2 Banks with X16 & X32 SDRAMs

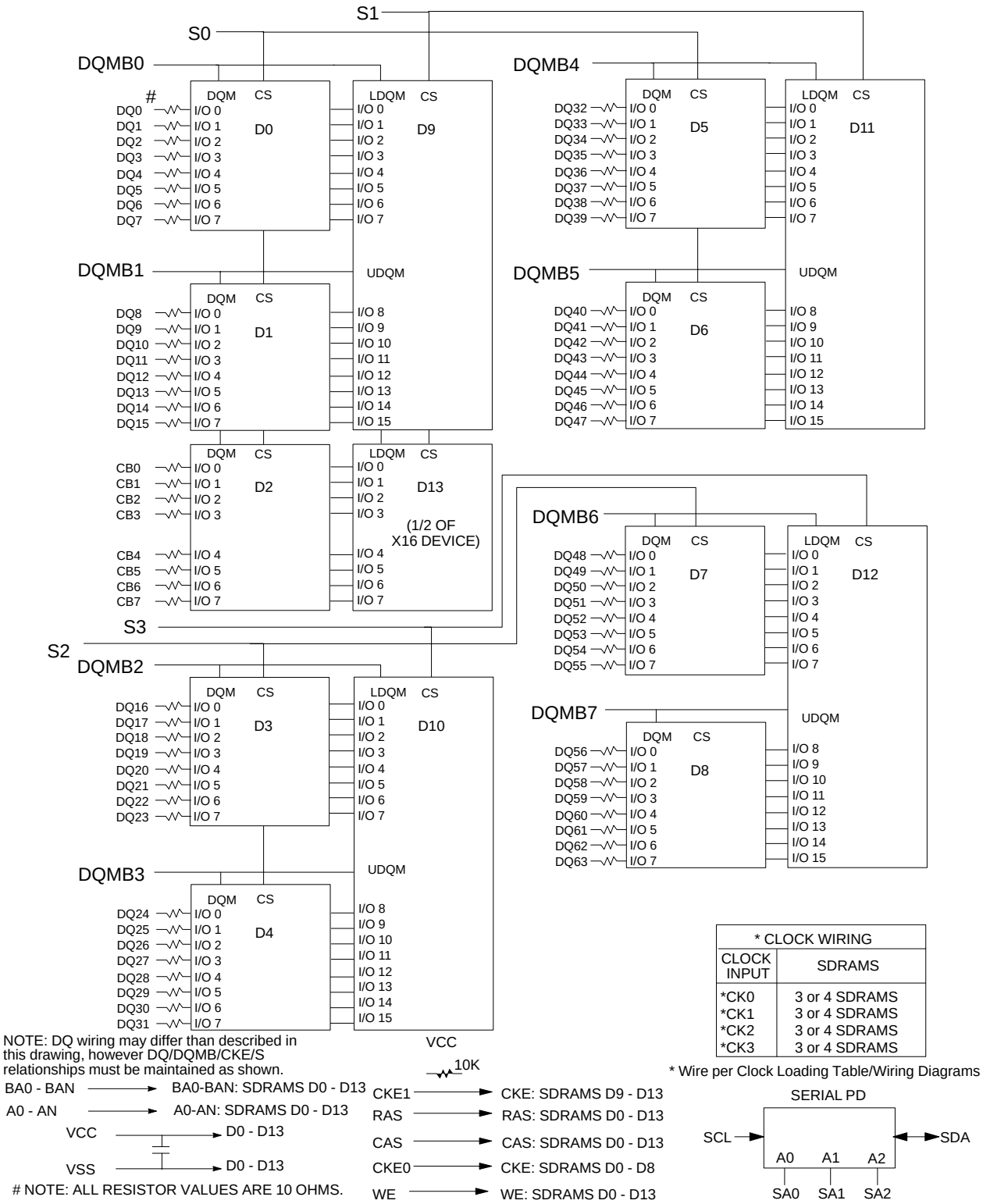
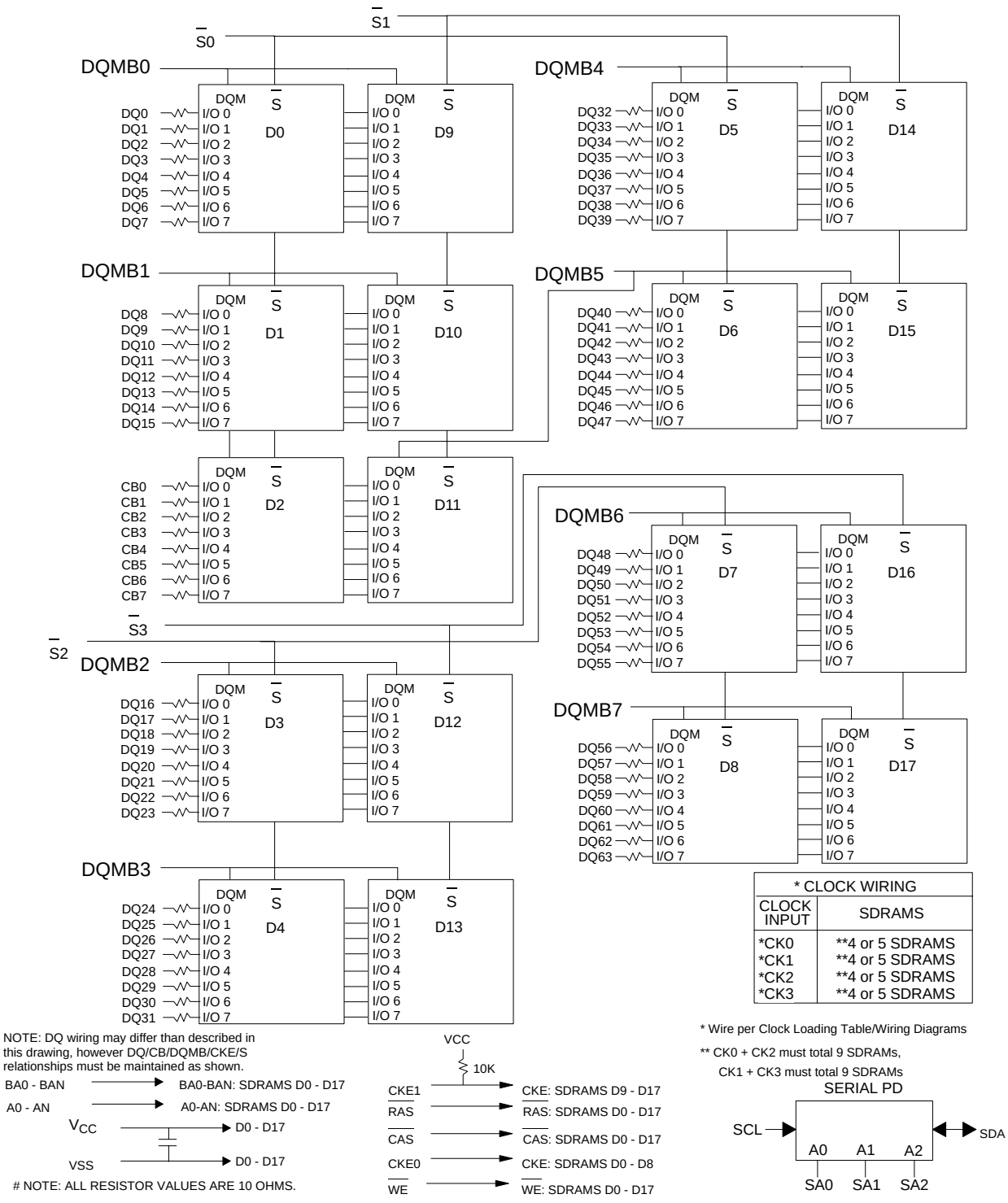


Figure 4.5.4–AB
X72 ECC SDRAM DIMM, 2 Banks with X8 & X16 SDRAMs



NOTE: All new designs for x8-based 2 bank 72 bit modules must be consistent with this diagram

Figure 4.5.4–AC
X72 ECC SDRAM DIMM, 2 Banks with X8 SDRAMs: Version 2

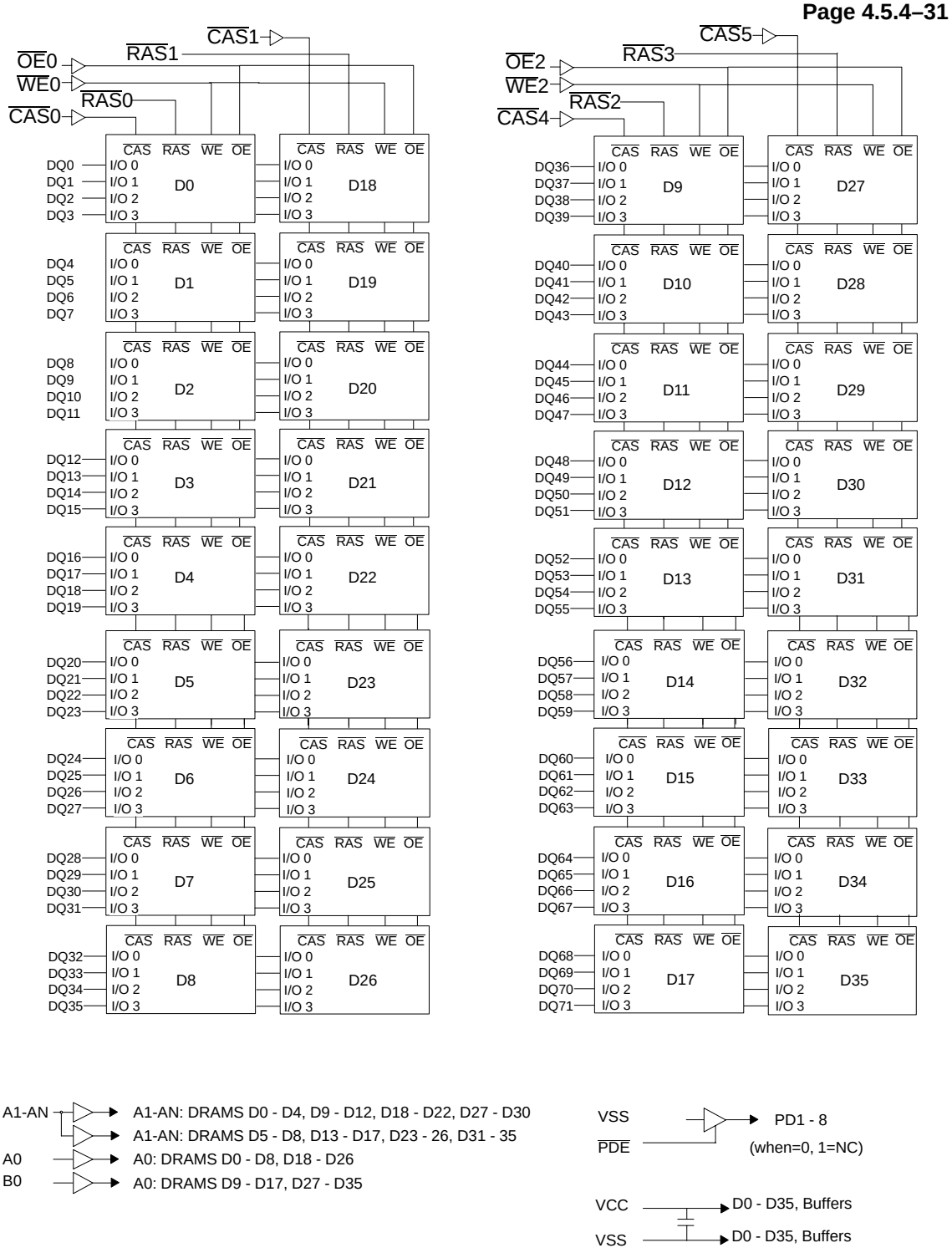


Figure AD
X72 ECC DIMM, 2 Bank with X4 DRAMs

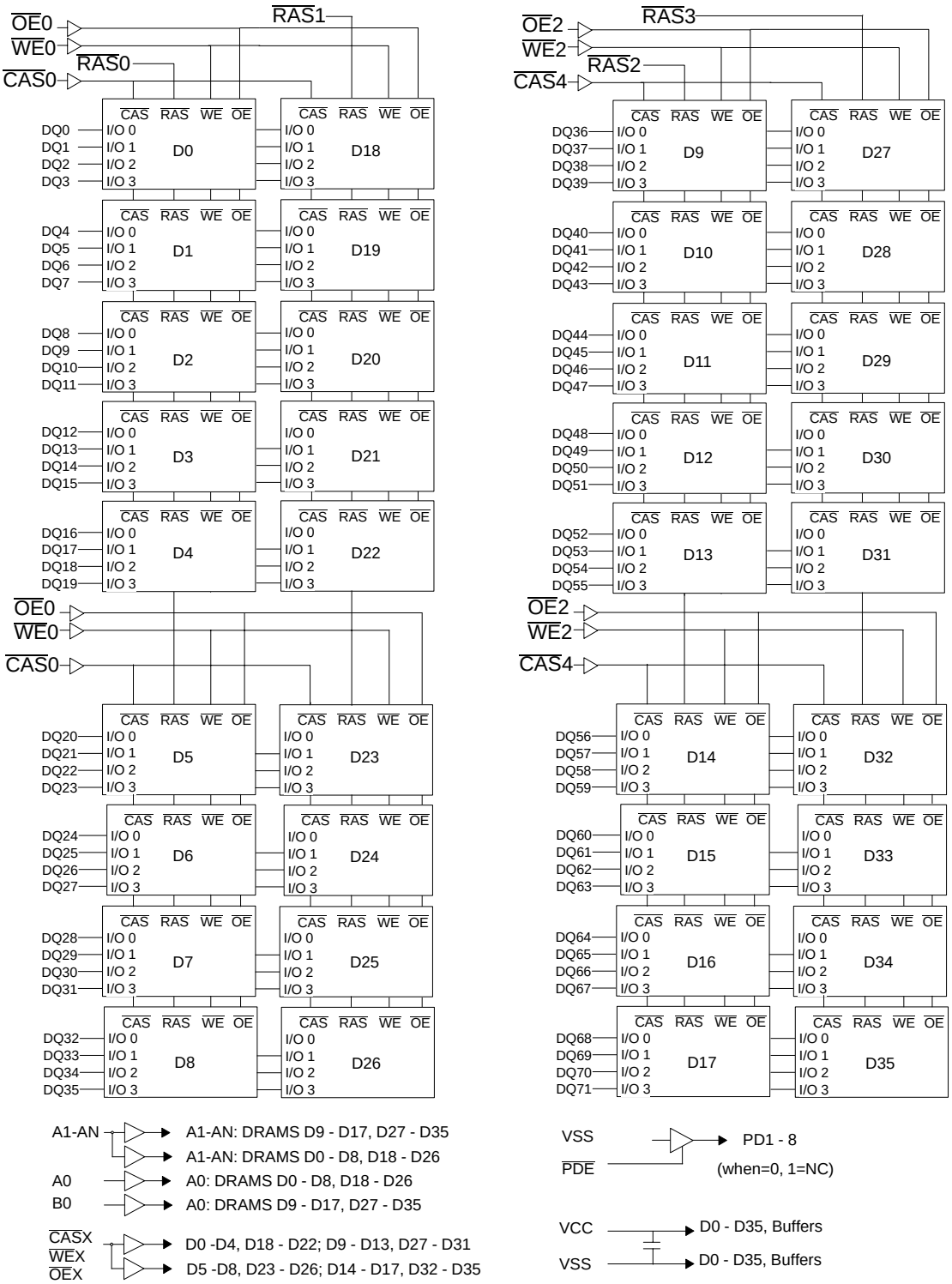
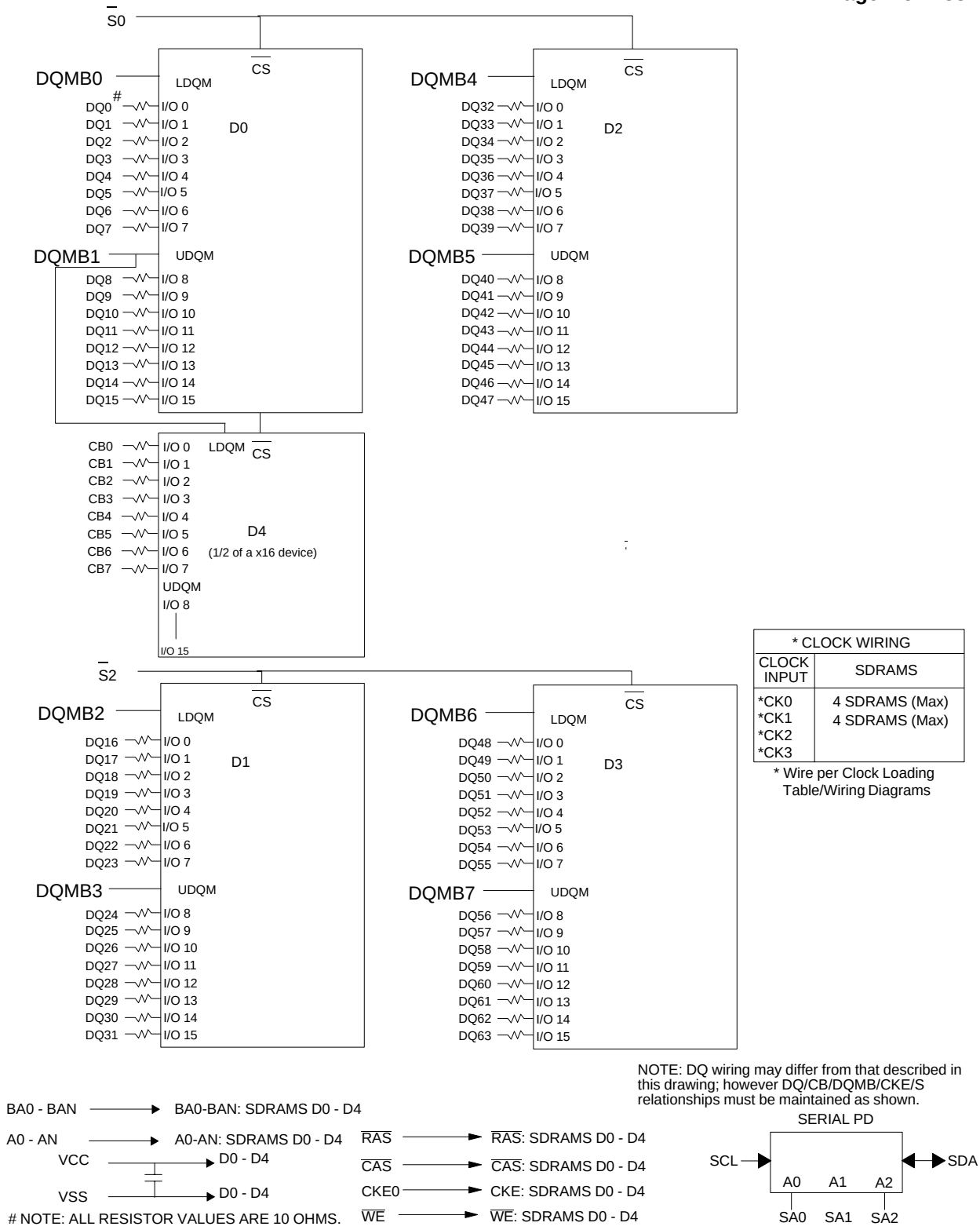


Figure AE

X72 ECC DIMM, 2 Bank with X4 DRAMs (Optimized for stacked DRAMs)



* CLOCK WIRING

CLOCK INPUT	SDRAMS
*CK0	4 SDRAMS (Max)
*CK1	4 SDRAMS (Max)
*CK2	
*CK3	

* Wire per Clock Loading Table/Wiring Diagrams

Figure AF
X72 ECC SDRAM DIMM, 1 Bank with X16 SDRAMs

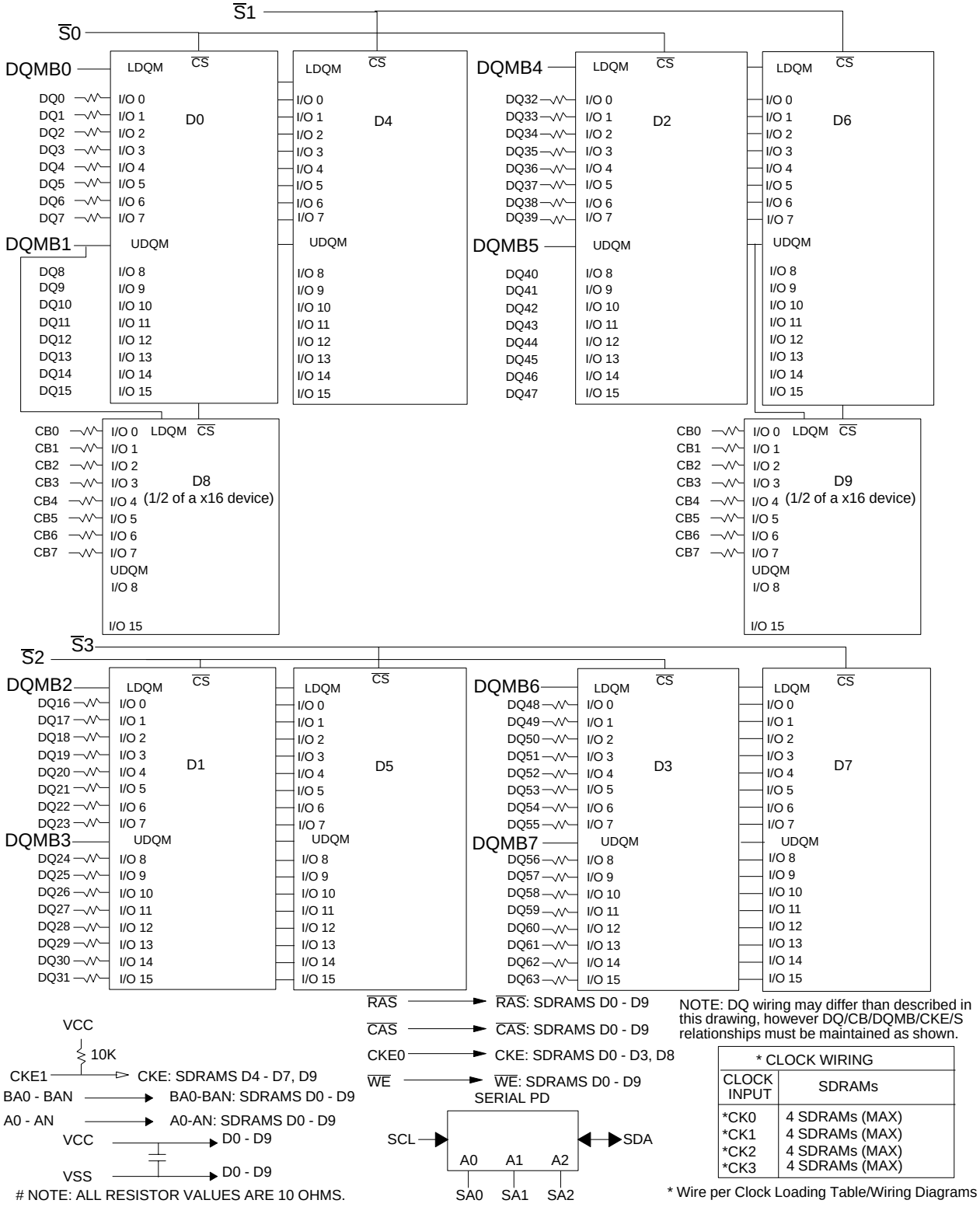


Figure AG
X72 ECC SDRAM DIMM, 2 Banks with X16 SDRAMs

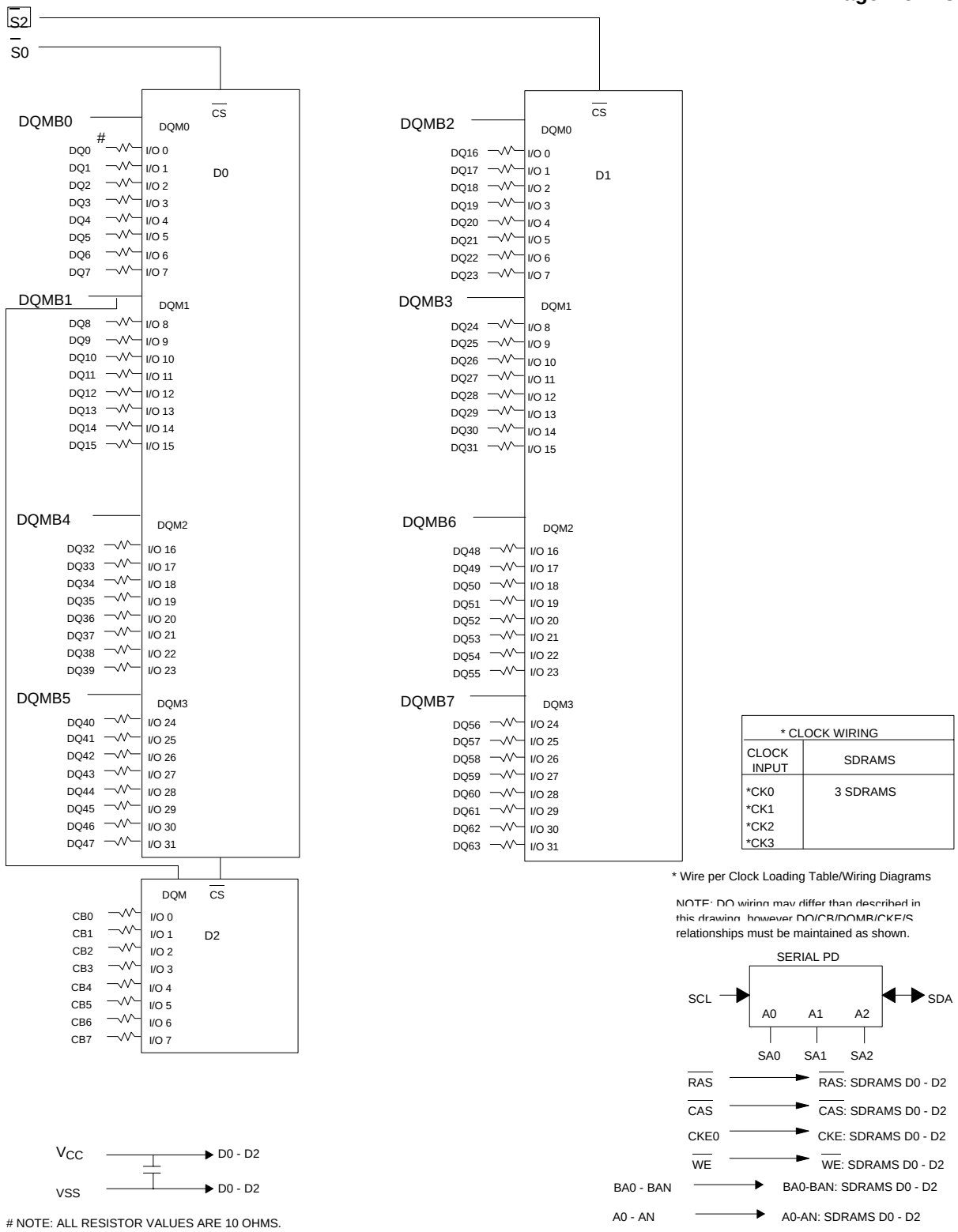


Figure AH
X72 SDRAM DIMM, 1 Bank with X32 & X8 SDRAM

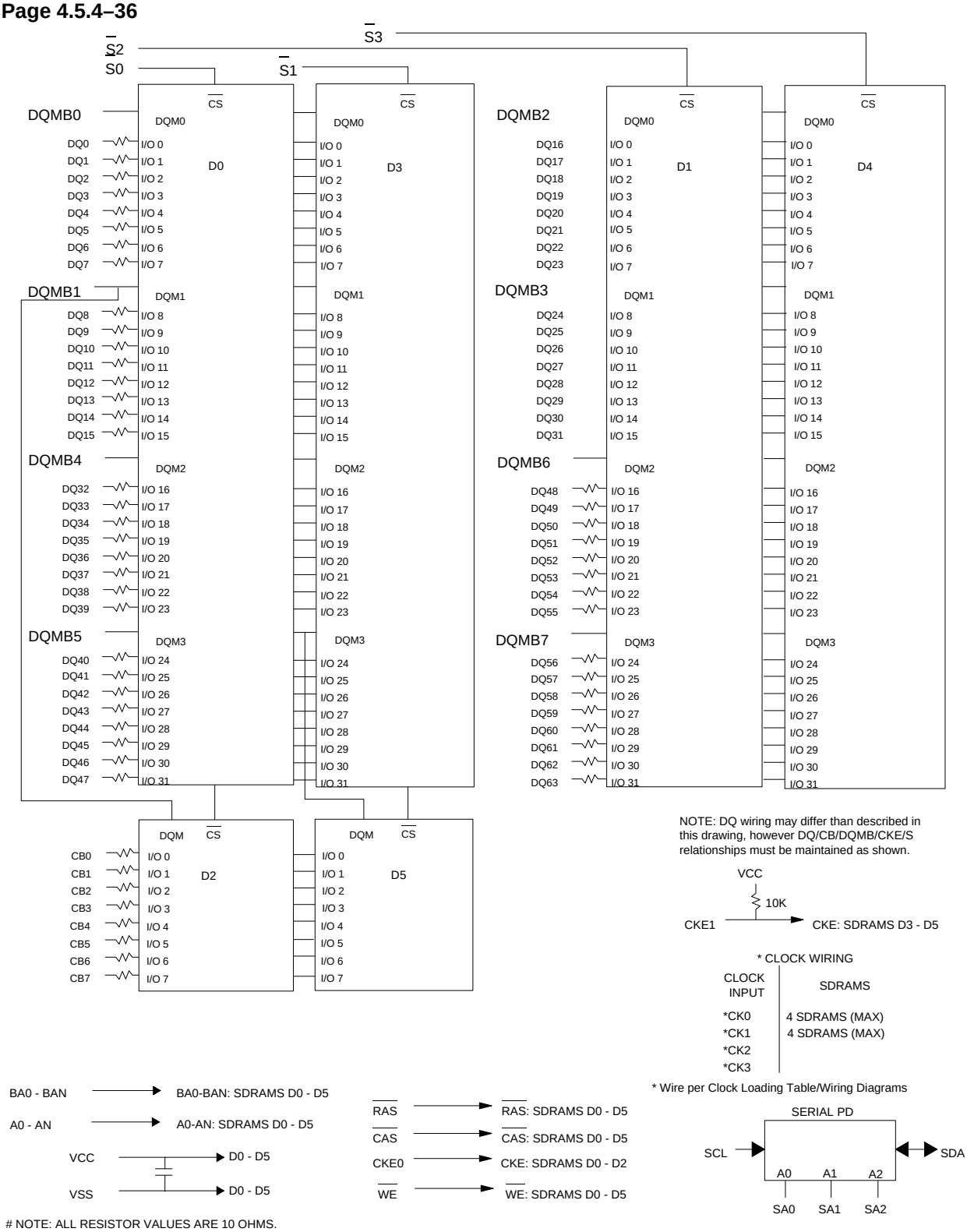


Figure AI
X72 SDRAM DIMM, 2 Banks with X32 & X8 SDRAMs

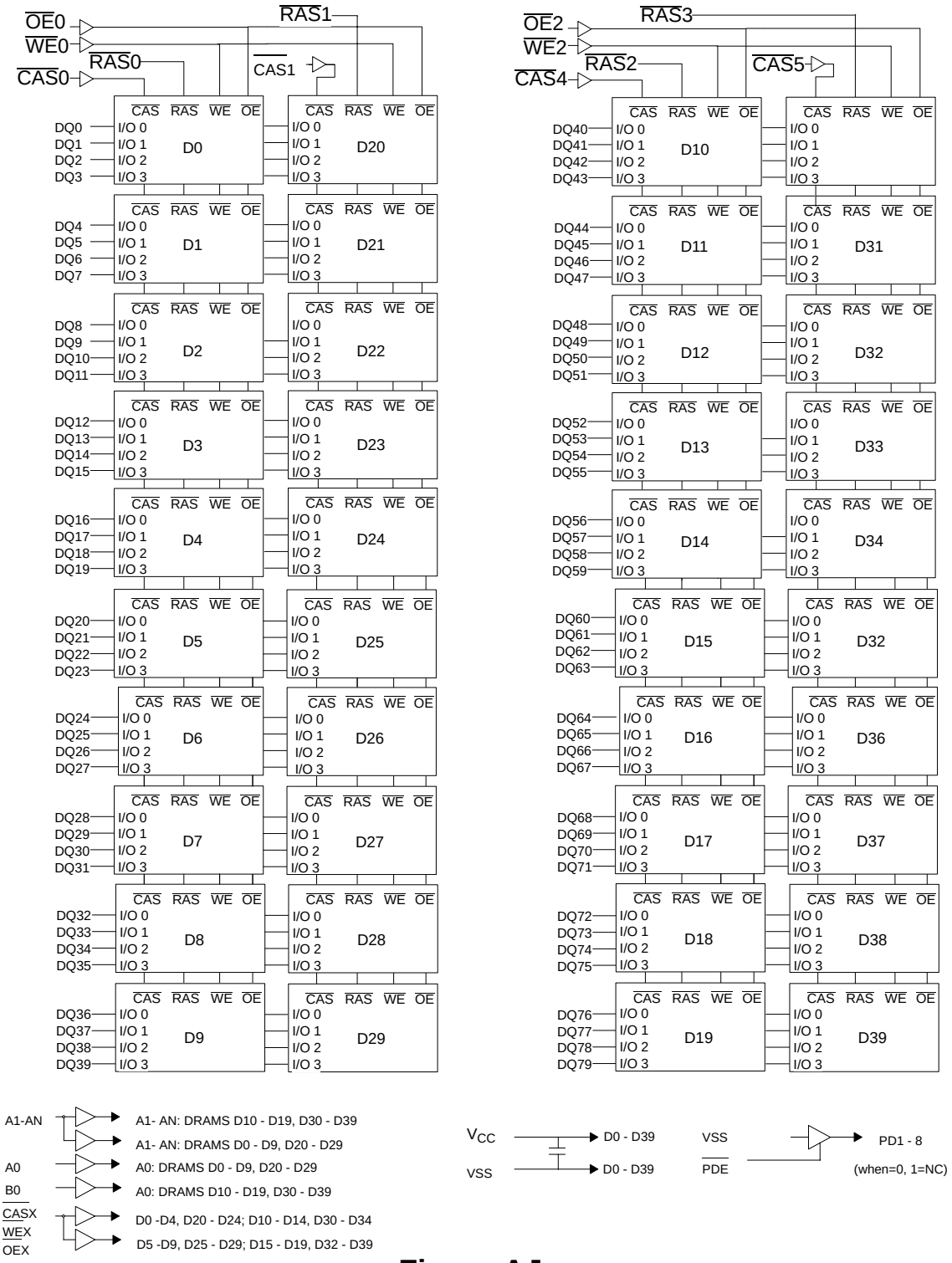


Figure AJ
X80 ECC DIMM, 2 Bank with X4 DRAMs

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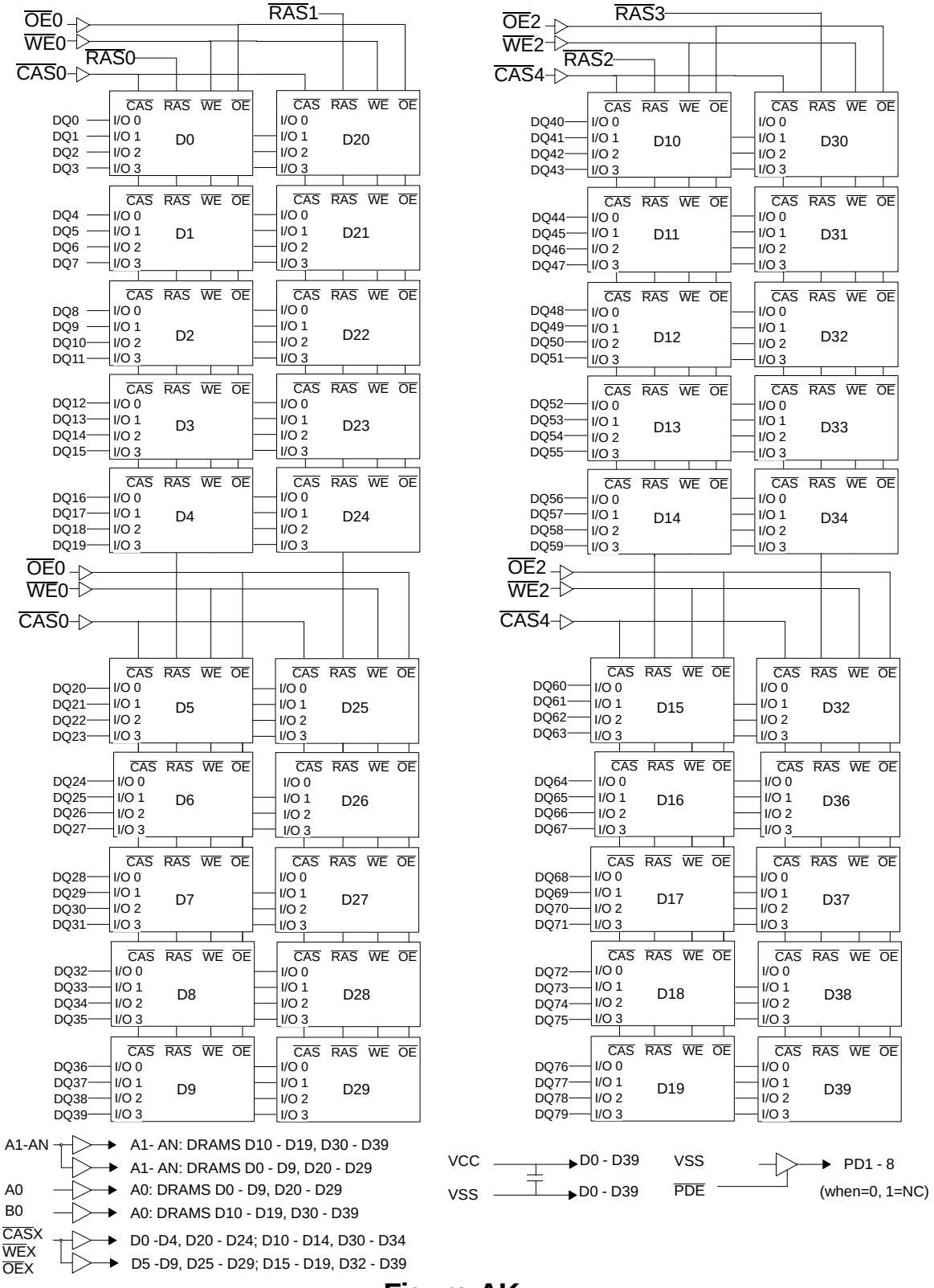

Figure AK
X80 ECC DIMM, 2 Banks with X4 DRAMs (Optimized for stacked DRAMs)